



STIC Search Report

EIC 2100

STIC Database Tracking Number: 121412

TO: Fred Ehichoya
Location: 4D4
Art Unit : 2172
Thursday, May 13, 2004

Case Serial Number: 09/992652

From: Carol Wong
Location: EIC 2100
PK2-4B33
Phone: 305-9729

carol.wong@uspto.gov

Search Notes

Dear Examiner Ehichoya,

Attached are the search results (from commercial databases) for your case.

Color tags mark the patents/articles which appear to be most relevant to the case. Pls review all documents, since untagged items might also be of interest. If you wish to order the complete text of any document, pls submit request(s) directly to the EIC2100 Reference Staff located in PK2-4B40.

Pls call if you have any questions or suggestions for additional terminology, or a different approach to searching the case. Finally, pls complete the attached Search Results Feedback Form, as the EIC/STIC is continually soliciting examiners' opinion of the search service.

Thanks,
Carol



File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)

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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200429

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Set	Items	Description
S1	77	JEDEC OR (JT OR JOINT)()ELECTRONIC?? ?()DEVICE? ? ()ENGINE- ER? ? OR JESD3()C OR JESD()3
S2	13754	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPL- DS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FGAS
S3	132165	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR- OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S4	102554	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S5	2295	S4(1W)LOGIC(1W)DEVICE? ?
S6	1739	S4(1W)LOGIC(1N)ARRAY? ?
S7	2230	S4(1W)GATE? ?(1W)ARRAY? ?
S8	122	S4() (IC OR ICS)
S9	501	S4(1W)INTEGRATED()CIRCUIT???? ?
S10	0	S4(1W)ELLECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S11	5	GENERIC(1W)ARRAY? ?(1W)LOGIC? ?
S12	14675	(READONLY OR READ()ONLY)(1W)(MEMORY? OR MEMORIES OR STORAG- E?)
S13	2152912	STORAGE? OR STORE? ? OR STORING OR MEMORY? OR MEMORIES OR - PRESTOR??? ?
S14	291957	S13(3N)(FIELD? ? OR SPACE? ? OR AREA? ? OR REGION? ? OR SE- CTOR? ? OR ZONE? ? OR SECTION? ? OR PART OR PARTS OR PORTION? ?)
S15	381480	S13(3N)DATA
S16	105618	S13(3N)(PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PRO- PERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATT- RIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR - FEATURES)
S17	0	S4(1W)ELECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S18	1940	BINARY(1W)TREE? ? OR HUFFMAN
S19	2991072	PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PROPERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATTRIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR FEATURES
S20	81323	S19(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACK- ED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDU- C? OR REDN? ? OR DIMINISH?)
S21	81569	S19(3N)(REDUC??? ? OR REDUCTION? OR DECREAS? OR DECREMENT? OR ENCOD??? ? OR CODIFY? OR CODIFIE? OR CODIFIC? OR INCOD??? - ?)
S22	413853	NONCONFORM? OR INCOMPAT? OR INOPERA? OR UNUSUAL OR DYSFUNC- T? OR INCOMPLETE? OR DEVIA? OR IRREGULAR? OR EXCEPTION? ? OR - DISTORT?
S23	447550	DISFUNCT? OR UNCONFORM? OR UNCOMPAT? OR UNCOMPLET? OR DISC- REPAN? OR DEGRAD? OR DISPARAT? OR BUG? ? OR ERROR? ? OR CORRU- PT? OR INVALID?
S24	3436179	MISTAK? OR FAIL???? ? OR PROBLEM? ? OR FAULT? OR DEFECT? OR DEFICIEN? OR ABNORMA? OR DAMAG? OR FLAW? OR IMPAIR?
S25	78162	ABERRA? OR MALFUNCTI? OR IMPERFECT?
S26	11523	DEBUG? OR DE()BUG???? ? OR ECC OR ECCS OR EDAC OR EDACS
S27	20	S4(1W)ELECTRICAL?? ?(1W)ERAS?(1W)LOGIC? ?
S28	232639	S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH- EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PRO- BING? OR SEARCH? OR SURVEY?)
S29	37450	S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? - OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR

LOCAT? OR REVIEW?)

S30 69353 S22:S25(3N) (DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENT-
IFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECO-
GNIS? OR RECOGNIZ? OR RECOGNIT?)

S31 252242 S22:S25(3N) (INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR
SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT???
? OR FILTER??? ?)

S32 62651 DATA(3N) (COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PAC-
KED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR RED-
UC? OR REDN? ? OR DIMINISH?)

S33 27090 DATA(3N) (DECREAS? OR DECREMENT? OR ENCOD???? ? OR CODIFY? -
OR CODIFIE? OR CODIFIC? OR INCOD??? ?)

S34 11 (S2:S3 OR S5:S12 OR S27) AND S1

S35 31558 (S2:S3 OR S5:S12 OR S27) AND S14:S16

S36 1663 S35 AND (S18 OR S20:S21 OR S32:S33)

S37 62 S36 AND S28:S31

S38 13 S36 AND S26

S39 0 S37 AND S1

S40 0 S36 AND S1

S41 0 S35 AND S1

S42 72 S37:S38

S43 220652 IC='H01L-027'

S44 46681 IC='H03K-019'

S45 4073 MC='U21-C01E'

S46 869 MC='U21-C01X'

S47 87507 IC='G06F-011'

S48 103373 IC='G06F-012'

S49 1619 MC='T01-G01A'

S50 83 S34 OR S37:S38

S51 22 S50 AND S43:S49

S52 22 IDPAT (sorted in duplicate/non-duplicate order)

S53 20 IDPAT (primary/non-duplicate records only)

S54 851 MC='W01-A02A'

S55 3499 MC='W02-J03B1'

S56 9366 MC='T01-D02'

S57 9410 IC='G06F-005'

S58 300204 IC='H04N-001'

S59 31135 IC='H03M-007'

S60 11 S50 AND S54:S59

S61 10 S60 NOT S51

S62 10 IDPAT (sorted in duplicate/non-duplicate order)

S63 9 IDPAT (primary/non-duplicate records only)

?

53/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015504430 **Image available**

WPI Acc No: 2003-566577/200353

XRPX Acc No: N03-450388

Content addressable memory functionality testing method in integrated circuits, tests memory array using read/write matching, priority encoding, match flag, invalidate data and valid data restricted search operations

Patent Assignee: AGERE SYSTEMS INC (AGER-N)

Inventor: HIGGINS F P; LEWANDOWSKI J L

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6543016	B1	20030401	US 99433759	A	19991104	200353 B

Priority Applications (No Type Date): US 99433759 A 19991104

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6543016	B1	23	G11C-029/00		

Abstract (Basic): US 6543016 B1

NOVELTY - The memory array is tested using the read/write operation, matching operation, priority encoding operation, match flag

operation and multiple match flag operation of the content addressable memory (CAM). The memory array is also **tested** using an **invalidate** data operation and a valid data restricted search operation.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for integrated circuit having a CAM system.

USE - For **testing** SRAM type **faults**, match faults, wild card faults, valid/invalid data faults in **memory** arrays e.g. flash electrically erasable programmable ROM, dynamic RAM and ROM, static RAM (SRAM), used in integrated circuit devices such as cellular telephones, answering machines, cordless telephones.

ADVANTAGE - Allows for efficiently combining the testing of the operations of content addressable memory and hence results in higher performance efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the CAM testing method.

pp; 23 DwgNo 2/4

Title Terms: CONTENT; ADDRESS; MEMORY; FUNCTION; TEST; METHOD; INTEGRATE; CIRCUIT; TEST; MEMORY; ARRAY; READ; WRITING; MATCH; PRIORITY; ENCODE; MATCH; FLAG; INVALID; DATA; VALID; DATA; RESTRICT; SEARCH; OPERATE

Derwent Class: S01; U14

International Patent Class (Main): G11C-029/00

International Patent Class (Additional): G06F-011/00

File Segment: EPI

Manual Codes (EPI/S-X): S01-G02B; U14-A05; U14-D; U14-D01B; U14-D03

53/9/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014389440 **Image available**

WPI Acc No: 2002-210143/200227

XRPX Acc No: N02-160554

Defect discovery method for memory, involves writing data in portion of memory area to be read out for analyzing and judging defective data and address lines

Patent Assignee: HITACHI LTD (HITA); HITACHI SCI SYSTEMS KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001243121	A	20010907	JP 200055950	A	20000228	200227 B

Priority Applications (No Type Date): JP 200055950 A 20000228

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001243121	A	10	G06F-012/16	

Abstract (Basic): JP 2001243121 A

NOVELTY - Several data lines and address lines are provided independently to a memory (6) mounted on a circuit board. Data is written-in a **portion of memory area** and then read out. Each read data is **analyzed** for judging **defective** data line or address line.

USE - For discovering defect in memory mounted on central processing unit (CPU) board.

ADVANTAGE - **Defect analysis** time is reduced and specific discovery of defective address line and data line is possible. Also write-in area can be reduced during defect discovery in CPU board and necessity of **data** elimination is **reduced**, thus **reducing data** elimination time.

DESCRIPTION OF DRAWING(S) - The figure shows the CPU board with

read only memory . (Drawing includes non-English language text).
Memory (6)
pp; 10 DwgNo 13/13
Title Terms: DEFECT; DISCOVER; METHOD; MEMORY; WRITING; DATA; PORTION;
MEMORY; AREA; READ; JUDGEMENT; DEFECT; DATA; ADDRESS; LINE
Derwent Class: S01; T01; U11; U13; U14
International Patent Class (Main): G06F-012/16
International Patent Class (Additional): G01R-031/28; G06F-011/22 ;
G11C-029/00
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01A1; T01-G02A; T01-H05B; U11-F01D2; U13-C07;
U14-D01

53/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013711261 **Image available**
WPI Acc No: 2001-195485/200120
XRPX Acc No: N01-139361

Programmable read only memory with built-in error correcting code,
has interruption controller which interrupts detection signal after which
corrected data is again written into memory cell

Patent Assignee: NEC IC MICROCOMPUTER SYSTEMS LTD (NIDE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001014226	A	20010119	JP 99182720	A	19990629	200120 B

Priority Applications (No Type Date): JP 99182720 A 19990629

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001014226	A		7 G06F-012/16	

Abstract (Basic): JP 2001014226 A

NOVELTY - An address latch (6) stores address for
writing-in/reading out of data into/or from memory cell, based on
which writing-in/reading-out are performed among memory cells. When
presence of inferior data is read-out from memory cell, error
detecting signal (12) is generated. Interruption controller interrupts
detecting signal and correction unit corrects inferior data and writes
corrected data into memory cell.

USE - Programmable read only memory (PROM) with built-in
error correcting code (ECC).

ADVANTAGE - As correction unit writes the corrected data again
into memory cell, after interruption of reduction signal, holder
for data correction is avoided, and hence reliability is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of
ECC built-in programmable read only memory .

Address latch (6)

Error detecting signal (12)

pp; 7 DwgNo 1/8

Title Terms: PROGRAM; READ; MEMORY; BUILD; ERROR; CORRECT; CODE; INTERRUPT;
CONTROL; INTERRUPT; DETECT; SIGNAL; AFTER; CORRECT; DATA; WRITING; MEMORY
; CELL

Derwent Class: T01; U21

International Patent Class (Main): G06F-012/16

International Patent Class (Additional): G06F-011/10

File Segment: EPI

Manual Codes (EPI/S-X): T01-G01A1; T01-H01C4; U21-A06

53/9/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013009557 **Image available**

WPI Acc No: 2000-181409/200016

XRPX Acc No: N00-133833

Programmable logic device for prototype system, emulation system of
debugging complex designs

Patent Assignee: ALTERA CORP (ALTE-N)

Inventor: NORMAN K A; PATEL R H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6020758	A	20000201	US 96615341	A	19960311	200016 B

Priority Applications (No Type Date): US 96615341 A 19960311

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6020758	A		8 H03K-019/173	

Abstract (Basic): US 6020758 A

NOVELTY - Logic components (100) coupled by an interconnecting network, contain memory cells (302) for storing configuration data . A configuration data line couples the memory cells to access transistors (304) forming a serial chain of data transmission. Data injection transistors (308) are respectively coupled to memory cells via partial reconfiguration (PR) data lines (312).

USE - For prototype system, emulation system of debugging complex designs and debugging system.

ADVANTAGE - Uses improved address wide programming that allows static or dynamic partial reconfiguration without disturbing the design function of the PLD . Provides data injection circuit that enables user to inject data into selected portion of the configuring host without affecting the PLD . Reduces number of data lines since data lines for two adjacent logic components are shared.

DESCRIPTION OF DRAWING(S) - The figure shows the alternative architecture drawing of the partially reconfigurable PLD .

Logic components (100)

Memory cells (302)

Access transistors (304)

Data injection transistors (308)

Partial reconfiguration data lines (312)

pp; 8 DwgNo 3/4

Title Terms: PROGRAM; LOGIC; DEVICE; PROTOTYPE; SYSTEM; EMULATION; SYSTEM;

DEBUG ; COMPLEX; DESIGN

Derwent Class: U21

International Patent Class (Main): H03K-019/173

International Patent Class (Additional): H03K-007/38

File Segment: EPI

Manual Codes (EPI/S-X): U21-C01E ; U21-C03D

53/9/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012923518 **Image available**

WPI Acc No: 2000-095354/200008

XRPX Acc No: N00-120438

Error correcting system in Reed-Solomon encoded data stream

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: COX C E; HASSNER M A

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SG 60153	A1	19990222	SG 974048	A	19971113	200008 B
US 6023782	A	20000208	US 96766681	A	19961213	200015

Priority Applications (No Type Date): US 96766681 A 19961213

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SG 60153	A1		42	G06F-011/08	
US 6023782	A		20	H03M-013/00	

Abstract (Basic): SG 60153 A

NOVELTY - An arithmetic unit iteratively generates intermediate and final values of coefficients of **error** locator polynomial and an **error evaluator** polynomial, where the coefficients are stored in random access memory. A control unit controls the arithmetic unit and the memory and detects the completion of the computation of the coefficients.

DETAILED DESCRIPTION - The bidirectional RAM (204) **stores** signals representing **data** elements and is coupled to operand register 1 (OP) (208) and multiplexer (MUX) (206) which selects between the output of RAM and OP (208) to determine the input to operand register 2 (OP) (210). The OPs are eight-bit registers with selectable load functions controlled by controller (228). The outputs of the OPs (208,210) are coupled to forcing circuits (212,214), respectively which selectively output either the input data stream or fixed data stream. The output of forcing circuit (212) is coupled to Galois field to multiplier which generates the product of two operands under Galois field. The two operands are supplied by forcing circuit (212) and MUX (220) which selects among the output of forcing circuit (214), output of accumulator (ACC) (222) and output of ROM (226) as controlled by the controller. The output of the multiplier is coupled to adder (202) whose other operand is supplied by the forcing circuit (214). The output of the adder is coupled to RAM and data is input into the RAM when the controller selects the input mode of the RAM. Inverse ROM (226) accepts its input from ACC, **stores** the **data** input and outputs the inverse, under the Galois field. The input of ACC is selected by MUX (218) from either output of forcing circuit (214) and adder (216), as controlled by the controller. The adder (216) accepts the output of inverse ROM (226) and output of ACC, as operands. The controller includes a state machine (240) which accepts input, generates output and controls the process. Five counters are used to control the execution flow. KCount (242) tracks the iterations through the main loop of the process. DCount (244) is used to resolve branch conditions in main loop of the process. LCount (246) is used as general loop counter. Shift index (248) outputs the count of shifts of **data** elements **stored** in the memory and interleave (250) keeps track of which interleave is being processed. TCount (276) indicates the correction power of the code to the state machine. The input signal start KES (278) initiates the process. Twelve control signals are output from state machine. RAM address (252) is the address into RAM (204) and RAM read (254) causes data element to be output. RAM write (256) causes write cycle to be performed to RAM (204). Load OP1 (258),

load OP2 (260) and load ACC (262) causes OP1 and OP2 and ACC to be loaded, respectively. Force OP1 (204) and force OP2 (266) cause the respective forcing circuits to output predetermined fixed data element. OMuxSelOp1 (268) and AMuxSelOp2 (270) causes the MUX (206) to select input coupled to OP1 (208) to be passed to OP2 (210) and causes the MUX (218) to the input coupled to forcing circuit (214) to be output to accumulator, respectively. MMuxSelOp2 (272) and MMuxSelInv (274) causes the MUX (220) to respectively select the input coupled to forcing circuit (214) and the input coupled to ROM (276) to be output to the multiplier.

USE - For solving key equation to decode the Reed-Solomon encoded data containing errors, used in communication and data storage applications.

ADVANTAGE - Considerable savings in hardware and cost is realized by eliminating the individual registers and storing all the intermediate variables in RAM or register file. Saving is achieved through the elimination of both the registers and the multiplexers to route the register contents to arithmetic units.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the error correcting system and controller.

Adder 202, 216 SRAM 204

MUX 206, 218, 220

OP 208, 210

Forcing circuits 212, 214

ACC 222

ROM 226

Controller 228

Counters 242, 244, 246, 276, 278

Index shift 248

Interleave 250

Control signals 252, 254, 256, 258, 260, 262, 264, 266, 268, 270, 272, 274

Dwg. 2a, 2b/

3

US 6023782 A

NOVELTY - An arithmetic unit iteratively generates intermediate and final values of coefficients of error locator polynomial and an error evaluator polynomial, where the coefficients are stored in random access memory. A control unit controls the arithmetic unit and the memory and detects the completion of the computation of the coefficients.

DETAILED DESCRIPTION - The bidirectional RAM (204) stores signals representing data elements and is coupled to operand register 1 (OP) (208) and multiplexer (MUX) (206) which selects between the output of RAM and OP (208) to determine the input to operand register 2 (OP) (210). The OPs are eight-bit registers with selectable load functions controlled by controller (228). The outputs of the OPs (208, 210) are coupled to forcing circuits (212, 214), respectively which selectively output either the input data stream or fixed data stream. The output of forcing circuit (212) is coupled to Galois field to multiplier which generates the product of two operands under Galois field. The two operands are supplied by forcing circuit (212) and MUX (220) which selects among the output of forcing circuit (214), output of accumulator (ACC) (222) and output of ROM (226) as controlled by the controller. The output of the multiplier is coupled to adder (202) whose other operand is supplied by the forcing circuit (214). The output of the adder is coupled to RAM and data is input into the RAM when the controller selects the input mode of the RAM. Inverse ROM (226) accepts its input from ACC, stores the data input and outputs the inverse, under the Galois field. The input of ACC is selected by MUX (218) from either output of forcing circuit (214) and adder (216), as controlled by the controller. The adder (216) accepts the output of

inverse ROM (226) and output of ACC, as operands. The controller includes a state machine (240) which accepts input, generates output and controls the process. Five counters are used to control the execution flow. KCount (242) tracks the iterations through the main loop of the process. DCount (244) is used to resolve branch conditions in main loop of the process. LCount (246) is used as general loop counter. Shift index (248) outputs the count of shifts of data elements stored in the memory and interleave (250) keeps track of which interleave is being processed. TCount (276) indicates the correction power of the code to the state machine. The input signal start KES (278) initiates the process. Twelve control signals are output from state machine. RAM address (252) is the address into RAM (204) and RAM read (254) causes data element to be output. RAM write (256) causes write cycle to be performed to RAM (204). Load OP1 (258), load OP2 (260) and load ACC (262) causes OP1 and OP2 and ACC to be loaded, respectively. Force OP1 (204) and force OP2 (266) cause the respective forcing circuits to output predetermined fixed data element. OMuxSelOp1 (268) and AMuxSelOp2 (270) causes the MUX (206) to select input coupled to OP1 (208) to be passed to OP2 (210) and causes the MUX (218) to the input coupled to forcing circuit (214) to be output to accumulator, respectively. MMuxSelOp2 (272) and MMuxSelInv (274) causes the MUX (220) to respectively select the input coupled to forcing circuit (214) and the input coupled to ROM (276) to be output to the multiplier.

USE - For solving key equation to decode the Reed-Solomon encoded data containing errors, used in communication and data storage applications.

ADVANTAGE - Considerable savings in hardware and cost is realized by eliminating the individual registers and storing all the intermediate variables in RAM or register file. Saving is achieved through the elimination of both the registers and the multiplexers to route the register contents to arithmetic units.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the error correcting system and controller.

Adder 202,216
 SRAM 204
 MUX 206,218,220
 OP 208,210 Forcing circuits 212,214
 ACC 222
 ROM 226
 Controller 228
 Counters 242,244,246,276,278
 Index shift 248
 Interleave 250
 Control signals 252,254,256,258,260,262,264,266,268,270,272,274
 Dwg.2a,2b/
 3

Title Terms: ERROR; CORRECT; SYSTEM; REED; ENCODE; DATA; STREAM

Derwent Class: T01; T03; U21

International Patent Class (Main): G06F-011/08 ; H03M-013/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-D01; T01-G01A ; T01-S01B; T03-A08A1C; T03-N01;
 T03-P01A; U21-A06

53/9/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011606826 **Image available**

WPI Acc No: 1998-023954/199803

XRPX Acc No: N98-018496

Memory holder device for TV - has EEPROM in which mirror image data is used for detecting and correcting errors in stored data

Patent Assignee: FUJITSU GENERAL LTD (GENH)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9282237	A	19971031	JP 9697937	A	19960419	199803 B

Priority Applications (No Type Date): JP 9697937 A 19960419

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 9282237 A 5 G06F-012/16

Abstract (Basic): JP 9282237 A

The device includes a micro computer (3) which receives data from a remote control (1) and are written to an EEPROM (2) based on a write-in controller (4a). The mirror image data are formed with stored data and checksum of stored data. The stored data and checksum are read from the EEPROM to micro computer based on read-out controller (4b). A main body with the mirror image data in the EEPROM detects and corrects errors in stored data.

ADVANTAGE - Provides normal data and operation, reduces EEPROM frequency, prolongs life of EEPROM, prevents malfunctioning by errors.

Dwg.1/3

Title Terms: MEMORY; HOLD; DEVICE; TELEVISION; EEPROM; MIRROR; IMAGE; DATA; DETECT; CORRECT; ERROR; STORAGE; DATA

Derwent Class: T01; U13; U14; U21

International Patent Class (Main): G06F-012/16

International Patent Class (Additional): G06F-011/10; G11C-029/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-G01A1; T01-H01C4; U13-C04B2; U14-A03B7; U14-D01B; U21-A06

53/9/7 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011516105 **Image available**

WPI Acc No: 1997-492591/199746

XRPX Acc No: N97-410037

Digital signal error detector for verifying operation of digital equipment - has comparator to which signal difference value signal and specified threshold value from limit register are input for generating error

Patent Assignee: TEKTRONIX INC (TEKT)

Inventor: ELKIND B

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2312534	A	19971029	GB 977988	A	19970421	199746 B
DE 19714976	A1	19971030	DE 1014976	A	19970410	199749
JP 10097439	A	19980414	JP 97106186	A	19970423	199825
US 5832003	A	19981103	US 96638057	A	19960425	199851
US 6119258	A	20000912	US 96638057	A	19960425	200046
			US 9847979	A	19980325	
GB 2312534	B	20010110	GB 977988	A	19970421	200103

Priority Applications (No Type Date): US 96638057 A 19960425; US 9847979 A 19980325

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2312534	A		17	G06F-007/64	
DE 19714976	A1		6	H04L-001/24	
JP 10097439	A		4	G06F-011/00	
US 5832003	A			G06F-011/00	
US 6119258	A			G01R-031/28	Cont of application US 96638057 Cont of patent US 5832003
GB 2312534	B			G06F-007/64	

Abstract (Basic): GB 2312534 A

The detector includes a difference generator (14) for producing a signal difference value signal from a repetitive input data signal and a reference data signal. A limit detector to which the signal difference value signal is input for generating an error signal when the signal difference value signal exceeds a specified threshold value. The limit detector (32) includes a limit register for **storing** the specified threshold **value**. A comparator (34) is provided to which the signal difference value signal and the specified threshold value from the limit register are input for generating the error signal when the signal difference value signal exceeds the specified threshold value.

A maximum register (16) **stores** a maximum threshold **value** as part of the specified threshold value. A minimum register (18) **stores** a minimum threshold **value** as part of the specified threshold value.

USE/ADVANTAGE - For processing **PAL** composite signals, **data compressed** signals or non-losses processed signals. Allows evaluating whether equipment is operating within acceptable margins of error or is seriously malfunctioning.

Dwg.1/1

Title Terms: DIGITAL; SIGNAL; ERROR; DETECT; VERIFICATION; OPERATE; DIGITAL ; EQUIPMENT; COMPARATOR; SIGNAL; DIFFER; VALUE; SIGNAL; SPECIFIED; THRESHOLD; VALUE; LIMIT; REGISTER; INPUT; GENERATE; ERROR

Derwent Class: T01; W02; W04

International Patent Class (Main): G01R-031/28; G06F-007/64; **G06F-011/00** ; H04L-001/24

International Patent Class (Additional): H04L-001/00; H04L-012/26; H04N-007/24; H04N-009/64; H04N-017/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-J08F; W02-F04A1; W02-F04A5; W04-P01A

53/9/8 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011030909 **Image available**

WPI Acc No: 1997-008833/199701

XRPX Acc No: N97-008044

Microcomputer-controller data storage method for e.g. rice cooker, air conditioner - involves writing data stored in RAM into electrically-erasable-programmable ROM only if power-failure signal is released by power-failure detector

Patent Assignee: RINNAI CORP (RINN)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8278923	A	19961022	JP 9578966	A	19950404	199701 B

Priority Applications (No Type Date): JP 9578966 A 19950404

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8278923	A		5	G06F-012/16	

Abstract (Basic): JP 8278923 A

The method begins by connecting a power-supply plug to a power-supply terminal (10) of a micro computer (1) to charge a back-up power supply unit (32). A power- failure detector (31) releases a power-failure signal during power failure.

The data to be written in a electrically-erasable-programmable ROM (12) of the microcomputer is stored in a RAM (13). The data stored in the RAM is written to the EEPROM only if the power-failure signal is released from the power- failure detector .

ADVANTAGE - Ensures utilisation of EEPROM for long time due to reduced data write-in frequency in EEPROM .

Dwg.1/2

Title Terms: MICROCOMPUTER; CONTROL; DATA; STORAGE; METHOD; RICE; COOKER; AIR; CONDITION; WRITING; DATA; STORAGE; RAM; ELECTRIC; ERASE; PROGRAM; ROM ; POWER; FAIL; SIGNAL; RELEASE; POWER; FAIL; DETECT

Derwent Class: P28; T01; X27

International Patent Class (Main): G06F-012/16

International Patent Class (Additional): A47J-027/00

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): T01-G03; T01-H01C4; T01-J08A; X27-C04; X27-E01B

53/9/9 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010862928 **Image available**

WPI Acc No: 1996-359879/199636

XRPX Acc No: N96-303425

Test data generation circuit for integrated circuit memory e.g. EEPROM , FLASHROM, SRAM - converts data signal output from test data memory to exclusive OR or its negative value with higher-order initial address message, from initial address message input through address line of test data memory

Patent Assignee: MITSUBISHI PLASTICS IND LTD (MISD)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8171518	A	19960702	JP 94313495	A	19941216	199636 B

Priority Applications (No Type Date): JP 94313495 A 19941216

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8171518	A		9	G06F-012/16	

Abstract (Basic): JP 8171518 A

The generation circuit has a test data memory (1) that stores a test data . A data signal output from the test data memory is converted to an exclusive OR or its negative value with a higher-order initial address message from an initial address message input through an address line of the test data memory , and is stored in a tested memory (2). The data read from the tested memory is compared with the converted data.

An abnormality is judged in the memory when the comparison data

are not the same. The higher order initial address message is input into a third memory from the initial address message input into the address line of the test **data memory**. The **data stored** previously is output. The data signal output from the test **data memory** is converted to the exclusive OR or its negative value with a data output from the third memory.

ADVANTAGE - Reduced mfg. cost and size. **Decreases** capacity of test **data memory**. Enables **detection** of memory **abnormality**.

Dwg.3/15

Title Terms: TEST; DATA; GENERATE; CIRCUIT; INTEGRATE; CIRCUIT; MEMORY; EEPROM ; SRAM; CONVERT; DATA; SIGNAL; OUTPUT; TEST; DATA; MEMORY; EXCLUDE ; NEGATIVE; VALUE; HIGH; ORDER; INITIAL; ADDRESS; MESSAGE; INITIAL; ADDRESS; MESSAGE; INPUT; THROUGH; ADDRESS; LINE; TEST; DATA; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-012/16

International Patent Class (Additional): G06F-011/22

File Segment: EPI

Manual Codes (EPI/S-X): T01-G02A2D; T01-H01

53/9/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010836641 **Image available**

WPI Acc No: 1996-333594/199633

Related WPI Acc No: 1996-041843

XRPX Acc No: N96-281184

Communication method for transferring data from mass storage device, e.g. CD- ROM to host computer - storing separated sectors of user and auxiliary data in contiguous memory blocks and performing error correction on all desired sectors before transferring to host computer via communications bus

Patent Assignee: OAK TECHNOLOGY INC (OAKT-N)

Inventor: VERINSKY P; WEDDLE G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5535327	A	19960709	US 94264600	A	19940623	199633 B
			US 95505557	A	19950721	

Priority Applications (No Type Date): US 95505557 A 19950721; US 94264600 A 19940623

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5535327	A	14	G06F-011/10	CIP of application	US 94264600

Abstract (Basic): US 5535327 A

The communication method involves reading a sector of user **data** from a mass **storage** device, e.g. a CD- ROM drive, separating the user data from the auxiliary **data** and **storing** each **portion** in a separate contiguous memory block. **Error detection** and correction is performed on the data which is then labelled with a block address.

Further sectors are read and processed in the same way until all the desired data has been transferred to memory blocks, using a different label for each sector. The error corrected user data is then transferred, over a communications bus, to a host computer. Pref. the auxiliary data read from the mass storage device is stored in the same memory block, replacing the previous auxiliary data block.

ADVANTAGE - Reduces amount of address storage required to locate

valid **data** blocks in DRAM. **Reduces** execution time required by system controller to address each user data block.

Dwg.2/5

Title Terms: COMMUNICATE; METHOD; TRANSFER; DATA; MASS; STORAGE; DEVICE; CD ; ROM ; HOST; COMPUTER; STORAGE; SEPARATE; SECTOR; USER; AUXILIARY; DATA ; CONTIGUOUS; MEMORY; BLOCK; PERFORMANCE; ERROR; CORRECT; SECTOR; TRANSFER; HOST; COMPUTER; COMMUNICATE; BUS

Index Terms/Additional Words: COMPACT; DISC; DRIVE

Derwent Class: T01; T03

International Patent Class (Main): G06F-011/10

International Patent Class (Additional): G06F-003/08; G11B-021/10

File Segment: EPI

Manual Codes (EPI/S-X): T01-C01; T01-G01A ; T03-B08; T03-N01

53/9/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010742106 **Image available**

WPI Acc No: 1996-239061/199624

Related WPI Acc No: 1994-341271

XPX Acc No: N96-200133

Flash EEPROM - has data controller contg. 2nd non-volatile memory for storing block bit map table corresp. to flash EEPROM block, and 3rd non-volatile memory for storing alternate address when redundant flash EEPROM is defective

Patent Assignee: HITACHI LTD (HITA)

Inventor: FUJITA K; NAKAO T; SAZE N; YAMAGATA H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5515333	A	19960507	US 92968334	A	19921029	199624 B
			US 94262314	A	19940617	

Priority Applications (No Type Date): JP 91282695 A 19911029

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5515333	A	10	G06F-011/00	Div ex application US 92968334	Div ex patent US 5359569

Abstract (Basic): US 5515333 A

The semiconductor memory includes an electrically rewritable non-volatile semiconductor **memory** . A **data** control circuit includes an **ECC** circuit and controls the writing and reading operations of data to and from the non-volatile semiconductor memory.

In order to temporarily hold data which is to be written into the non-volatile semiconductor memory, a volatile cache semiconductor memory is used. This volatile cache semiconductor memory has a storage capacity which is equal to or less than the storage capacity of the non-volatile semiconductor **memory** itself. A **data** control circuit is also provided to read out data from the non-volatile semiconductor memory and the volatile cache semiconductor memory, and to transfer the data from the volatile semiconductor to the non-volatile semiconductor memory.

ADVANTAGE - Improved efficiency and life, low cost and high **data** access speed. **Decreases** number of commands of combining small data volumes in data write operation. Data re-writing separation can be executed at high speed without knowledge of block as rewriting unit of data.

Dwg.1,5/9

Title Terms: FLASH; **EEPROM** ; DATA; CONTROL; CONTAIN; NON; VOLATILE; MEMORY ; STORAGE; BLOCK; BIT; MAP; TABLE; CORRESPOND; FLASH; **EEPROM** ; BLOCK; NON; VOLATILE; MEMORY; STORAGE; ALTERNATE; ADDRESS; FLASH; **EEPROM** ; DEFECT

Derwent Class: T01; U14

International Patent Class (Main): **G06F-011/00**

File Segment: EPI

Manual Codes (EPI/S-X): T01-G03; T01-H01B3; T01-H03A; U14-A07

53/9/12 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010691059 **Image available**

WPI Acc No: 1996-188015/199619

Related WPI Acc No: 1993-405247; 1995-115083

XRFX Acc No: N96-157311

Determining encoding scheme in mixed data encoding scheme for programming data into sector of flash **EEPROM** system - encoding and storing **ECC** for part of data, retrieving part of data and **ECC** by assuming either data encoding , decoding **ECC** and determining data in group has been programmed using assumed data encoding when **ECC** error is absent

Patent Assignee: SANDISK CORP (SAND-N)

Inventor: GROSS S J; GUTERMAN D C; HARARI E; MEHROTRA S; NORMAN R D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5504760	A	19960402	US 91670246	A	19910315	199619 B
			US 93148930	A	19931108	

Priority Applications (No Type Date): US 93148930 A 19931108; US 91670246 A 19910315

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5504760	A	26	G06F-011/10		CIP of application US 91670246 CIP of patent US 5270979

Abstract (Basic): US 5504760 A

An array of **EEPROM** memory cells are organised into groups of cells, each group having data programmed according to either first **data encoding** or a second **data encoding** . The first **data encoding** has 1st and 2nd logical states of data represented respectively by the erased state and the programmed state. The second **data encoding** has the representations of the first and second logical states reversed relative to the programmed and erased states of the first **data encoding** .

In a read operation on a group, it is determined whether the data has been programmed according to the 1st or the 2nd **data encoding** . When **data** is programmed into the group, an error correction code ('**ECC** ') is encoded and **stored** for **part** of the data.

In a subsequent read operation on the group, the part of the data and the **ECC** are retrieved by assuming either the first or the second **data encoding** . The **ECC** is decoded for the part of the data. It is determined that the data in the group has been programmed using the assumed **data encoding** when a first condition is true that an **ECC** error is absent.

ADVANTAGE - Improves performance of erasing and programming of

EEPROM system, while minimising stress and maximising performance, maintaining optimum erase parameters during history of EEPROM program-erase cycling.

Dwg.14a/15

Title Terms: DETERMINE; ENCODE; SCHEME; MIX; DATA; ENCODE; SCHEME; PROGRAM; DATA; SECTOR; FLASH; EEPROM ; SYSTEM; ENCODE; STORAGE; ECC ; PART; DATA ; RETRIEVAL; PART; DATA; ECC ; ASSUME; DATA; ENCODE; DECODE; ECC ; DETERMINE; DATA; GROUP; PROGRAM; ASSUME; DATA; ENCODE; ECC ; ERROR; ABSENCE

Derwent Class: T01; U13; U14

International Patent Class (Main): G06F-011/10

File Segment: EPI

Manual Codes (EPI/S-X): T01-D02; T01-G01A ; U13-C04B2; U14-D02

53/9/13 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010356179 **Image available**

WPI Acc No: 1995-257493/199534

Memory module for extension for image processing part of high quality printer - has two 16M ROMs and multiple 4M DRAMs which are mounted on same substrate

Patent Assignee: CANON KK (CANO)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 7160384	A	19950623	JP 93338790	A	19931202	199534 B

Priority Applications (No Type Date): JP 93338790 A 19931202

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 7160384	A	4	G06F-003/00	

Abstract (Basic): JP 7160384 A

The memory module consists of two 16M ROMs (31a, 31b) and multiple 4M DRAMs (22 - 29) mounted on same surface. In the ROMs control programmes are stored. The specification of the image processing part and the connector part (21) of the extension memory module is same as that of the specification of the connector of the 72-pin DRAM module defined by JEDEC .

USE/ADVANTAGE - In e.g. printer of laser beam system. Plans miniaturisation of image processing part and curtailment of electronic components.

Dwg.1/4

Title Terms: MEMORY; MODULE; EXTEND; IMAGE; PROCESS; PART; HIGH; QUALITY; PRINT; TWO; ROM ; MULTIPLE; MOUNT; SUBSTRATE

Index Terms/Additional Words: MEMORY; MODULE; EXTEND; IMAGE; P

Derwent Class: T01; T04

International Patent Class (Main): G06F-003/00

International Patent Class (Additional): G06F-012/00 ; G11C-005/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-H01B1; T04-G04A

53/9/14 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009325831 **Image available**

WPI Acc No: 1993-019294/199303

XRPX Acc No: N93-014792

Error correction system for semiconductor memory - uses syndrome signal to provide correction signal for each stored data group

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)

Inventor: KOHDA K; MAKIHARA H

Number of Countries: 004 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4220196	A1	19930114	DE 4220196	A	19920619	199303 B
JP 5002898	A	19930108	JP 91151809	A	19910624	199306
US 5383205	A	19950117	US 92894661	A	19920605	199509
DE 4220196	C2	19950406	DE 4220196	A	19920619	199518
KR 9510311	B1	19950914	KR 9210893	A	19920623	199846

Priority Applications (No Type Date): JP 91151809 A 19910624

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4220196	A1		35	G11C-029/00	
US 5383205	A		33	G06F-011/10	
DE 4220196	C2		35	G11C-029/00	
JP 5002898	A			G11C-029/00	
KR 9510311	B1			G11C-029/00	

Abstract (Basic): DE 4220196 A

The error correction system uses a correction circuit for error correction via Hamming matrix operation. Each **memory field** holds quantity of data divided into 2 data groups and priority data, used with these data groups to provide syndrome signals via a syndrome signal generator.

A correction signal generator sequentially provides correction signals for the two data groups in synchronism with the operation of a data group selector, in response to the supplied syndrome signal, with corresponding correction of the **stored data** via a **data** correction stage.

USE - For **read only** semiconductor **memory** .

Dwg.1/22

Abstract (Equivalent): DE 4220196 C

The semiconductor device has a **memory** cell field (1,2) with **stored data** (d0-d31) and also parity data (PO-P5), a unit (8) for reading data from the cells, a unit (11) for correcting an error in the data and an operation corresponding to a pre-determined Hamming matrix is applied to the data.

The data (d0-d31) in the unit (11) is divided uniformly into two halves (d0-d15; d16-d31), forming two groups. This unit contains a unit for producing a number of syndrome signals on the basis of the two groups and the parity data, a group selector unit, a correction signal producing unit and finally a data correcting unit.

USE/ADVANTAGE - Suitable for semiconductor memorised. Employs Hamming matrix for correcting **data** , **reducing** size of correction circuit.

Dwg.1/22

Abstract (Equivalent): US 5383205 A

The mask **ROM** has an **ECC** (error correction circuit) for carrying out operation according to a Hamming matrix in which all but 2 of 6 elements in one column and the other column match each other. The columns correspond to 32 data that will be provided to an external source, and the one column corresponds to the other column by 16

columns.

The ECC is implemented so that one half of 32 correction signals with which exclusive ORs are to be taken with 32 data, are generated by a circuit identical to that of a circuit for generating the other half of the 32 correction signals; and the circuit for taking the exclusive ORs from one half of the 32 data and the corresponding correction signals can be used for taking exclusive ORs from the remaining half of the 32 data and the corresponding correction signals.

ADVANTAGE - Number of component elements for correction signal generator and for data correction circuit, and number of input signal lines to data correction circuit are reduced to half, alleviating circuit complexity of entire ECC in comparison with that of conventional one.

Dwg.1,2/22

Title Terms: ERROR; CORRECT; SYSTEM; SEMICONDUCTOR; MEMORY; SYNDROME; SIGNAL; CORRECT; SIGNAL; STORAGE; DATA; GROUP

Derwent Class: U14

International Patent Class (Main): G06F-011/10 ; G11C-029/00

International Patent Class (Additional): G06F-012/16 ; H01L-027/10

File Segment: EPI

Manual Codes (EPI/S-X): U14-D02

53/9/15 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007288809

WPI Acc No: 1987-285816/198741

XRPX Acc No: N87-214223

Encoder and error corrector for BCH code - delays input data while syndrome computer and ROM develop correcting pulse for injection on timed release

Patent Assignee: KENWOOD KK (TRIR)

Inventor: KOBAYASHI H; SHIRAISHI K

Number of Countries: 002 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 240921	A	19871014	EP 87104823	A	19870401	198741 B
JP 62233932	A	19871014	JP 8675549	A	19860403	198747
EP 240921	B1	19940727	EP 87104823	A	19870401	199429
DE 3750269	G	19940901	DE 3750269	A	19870401	199434
			EP 87104823	A	19870401	

Priority Applications (No Type Date): JP 8675549 A 19860403

Cited Patents: A3...8917; No-SR.Pub; US 3714629; US 4107652; 01Jnl.Ref

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 240921 A E 13

Designated States (Regional): DE

EP 240921 B1 E 7 H03M-013/00

Designated States (Regional): DE

DE 3750269 G H03M-013/00 Based on patent EP 240921

Abstract (Basic): EP 240921 A

Input data applied to the coder is delayed in a shift register (2) whilst simultaneously processed in a syndrome computer (1) to identify errors. The resulting computer output is latched (3) and applied as an address to a ROM (4) which stores error position data. From the ROM (4), the resulting output is handled by an up-counter unit

(5), under control of a timing generator (7), which initiates a count to a preset level. At this level, a ripple carry is executed and is used as an error correcting signal.

Timing of the up-counter (5) operation is synchronised by the timing generator (7) with the release of the input data held in the delay register (2). Both signals are applied to an EXOR gate (6) so that its **encoded data** output is corrected by injection of the ripple carry pulse at the appropriate point.

ADVANTAGE - Post - ROM circuitry is simpler, and medium scale integration is therefore simplified.

1/2

Abstract (Equivalent): EP 240921 B

A BCH code signal correcting system including means (1, 3, 4) for generating error position data derived from a syndrome in an input BCH code signal, and correction means (6) for correcting the error in the input code signal; wherein the input code signal data are further processed in a serial bit stream; the correcting system comprising means (5, 7) responsive to the error position data for producing a timing signal in dependence on a time interval between the error position and a reference position in the input BCH code signal; and means (2) for delaying the input BCH code signal so that said timing signal timely corresponds to the error position in the delayed input BCH code signal; wherein said correction means (6) is responsive to the timing signal and the delayed input code signal for correcting the error in the delayed input code signal; characterised in that said error position generating means (1, 3, 4) includes memory means (4) for storing error position binary code data addressed by the syndrome in the input BCH code signal, and said timing signal producing means (5, 7) includes a counter (5) responsive to a load signal for being preset by the error position binary code data read out from said memory means (4) and responsive to a clock signal for counting until a reference count to produce the timing signal; said timing signal being a carry signal.

(Dwg.1/2f)

Title Terms: ENCODE; ERROR; CORRECT; BCH; CODE; DELAY; INPUT; DATA; SYNDROME; COMPUTER; ROM; DEVELOP; CORRECT; PULSE; INJECTION; TIME; RELEASE

Index Terms/Additional Words: BOSE

Derwent Class: T01; U21

International Patent Class (Main): H03M-013/00

International Patent Class (Additional): G06F-011/10

File Segment: EPI

Manual Codes (EPI/S-X): T01-G01; U21-A06

53/9/16 (Item 16 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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004250916

WPI Acc No: 1985-077794/198513

Compact hybrid integrated circuit device increasing packing density - has UV- EPROM and other element hybridised to use package standardised by JEDEC without UV rays blocking seal NoAbstract Dwg 2/5

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 60030171	A	19850215	JP 83138477	A	19830728	198513 B

Priority Applications (No Type Date): JP 83138477 A 19830728

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 60030171 A 3

Title Terms: COMPACT; HYBRID; INTEGRATE; CIRCUIT; DEVICE; INCREASE; PACK;
DENSITY; ULTRAVIOLET; EPROM ; ELEMENT; HYBRID; PACKAGE; STANDARD;
ULTRAVIOLET; RAY; BLOCK; SEAL; NOABSTRACT

Derwent Class: U14

International Patent Class (Additional): H01L-027/10

File Segment: EPI

Manual Codes (EPI/S-X): U14-A06A; U14-H03

53/9/17 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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004246043

WPI Acc No: 1985-072921/198512

XRPX Acc No: N85-054381

Logic circuit prodn. flaws automatic search appts. - has controlled
pre-analyser with outputs to data memory and to points switch
connected to circuit on test

Patent Assignee: VINNITSK POLY (VINN-R); VINNITSK TERMINAL (VINN-R)

Inventor: BAIDA N P; SEMERENKO V P; SHPILEVOI V T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SU 1108451	A	19840815	SU 3480480	A	19820811	198512 B

Priority Applications (No Type Date): SU 3480480 A 19820811

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

SU 1108451 A 30

Abstract (Basic): SU 1108451 A

The appts. contg. a memory with address selector (2), output signal discriminator (7), comparator (11), and a control circuit, has a points switch (4), initial condition (5), compressed standard signal (9) and compressed output signal (10) registers, pre-analyser (6), compressed data read - only memory (10), text rendition unit (12), modulo-2 adder (13) and the Start button (16), and the control circuit (15) is reconstructed.

Test points of the logic circuit (18) on test are connected cyclically by the points switch. Logical constants of initial conditions are sotred during the test. The pre-analyser contains seven counters, three comparators and other parts for checking on non-logical flaws since the circuit on test has a limited number of components, less memory capacity is required to store tests for the individual components than a memory storing a full test for all the logic circuit.

USE/ADVANTAGE - In prodn. testing of assembled printed units contg. digital integrated circuits, all the non-logical flaws are eliminated before rated voltage is applied to search for logical flaws , so ensuring non-destructive testing and widening the field of application. A search is made for faults in greater depth and a memory of less capacity can be used. Bul.30/15.8.84. (30pp Dwg.No.1/11)

Title Terms: LOGIC; CIRCUIT; PRODUCE; FLAW; AUTOMATIC; SEARCH; APPARATUS;
CONTROL; PRE; ANALYSE; OUTPUT; DATA; MEMORY; POINT; SWITCH; CONNECT;
CIRCUIT; TEST

Derwent Class: S01; T01; U11

International Patent Class (Additional): G06F-011/00
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01A; T01-G02; U11-F01D

53/9/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
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06354785 **Image available**
1 CHIP MICROCOMPUTER

PUB. NO.: 11-296392 [JP 11296392 A]
PUBLISHED: October 29, 1999 (19991029)
INVENTOR(s): FUKUSHIMA KIYOSHI
APPLICANT(s): NEC CORP
APPL. NO.: 10-097287 [JP 9897287]
FILED: April 09, 1998 (19980409)
INTL CLASS: G06F-011/10 ; G06F-012/16 ; G06F-015/78

ABSTRACT

PROBLEM TO BE SOLVED: To provide a 1 chip microcomputer for reducing the work load on a user at the time of preparing ECC (error collection code) data, preventing increase of an EEPROM (electrical erasable programmable read only memory) writing time based on the ECC data, and reducing a memory capacity.

SOLUTION: This 1 chip microcomputer is provided with a firm ROM 5 for storing a program for generating ECC data from user data and an EEPROM control circuit 7 for controlling wiring of user data and the ECC data in an EEPROM 8. A CPU 2 stores the ECC data generated by the program of the firm ROM 5 from the user data and the original user data in a user data area 83 and an ECC data area 84 of the EEPROM 8 according to the control of the EEPROM control circuit 7, and reads the user data in the user data area 83 and the ECC data in the ECC data area 84 for successively operating an error correction processing.

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53/9/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO
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06341107 **Image available**
DEVELOPMENT SUPPORTING DEVICE FOR SOFTWARE

PUB. NO.: 11-282711 [JP 11282711 A]
PUBLISHED: October 15, 1999 (19991015)
INVENTOR(s): TAKAMATSU SHIRO
APPLICANT(s): TOSHIBA MICROELECTRONICS CORP
TOSHIBA CORP
APPL. NO.: 10-081649 [JP 9881649]
FILED: March 27, 1998 (19980327)
INTL CLASS: G06F-011/22 ; G06F-011/28

ABSTRACT

PROBLEM TO BE SOLVED: To enable a debug to restart from a state in which a power source is disconnected, to eliminate a limit of the number of data writing and to reduce a time needed for loading data.

SOLUTION: This development supporting device 11 for software is equipped with an emulation memory part 14 for emulating an EEPROM 12c built in a micro controller unit 12, and an emulation memory part 14 is composed of an SRAM 14c for storing data which are to be written into the EEPROM 12c, a timer 14f for making a busy time which generates at the time of writing into the EEPROM 12c and a power source backup circuit 14a for storing the data in the SRAM 14c. According to this structure, since the data of the SRAM 14c are retained even after the power source is disconnected, the debug can be easily restarted from the state at the time of power source disconnection.

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53/9/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO
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03982651 **Image available**
SEMICONDUCTOR MEMORY DEVICE

PUB. NO.: 04-347751 [JP 4347751 A]
PUBLISHED: December 02, 1992 (19921202)
INVENTOR(s): ENDO KANICHI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-120418 [JP 91120418]
FILED: May 24, 1991 (19910524)
INTL CLASS: [5] G06F-012/16 ; G06F-011/10
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1525, Vol. 17, No. 207, Pg. 72, April 22, 1993 (19930422)

ABSTRACT

PURPOSE: To supply a semiconductor memory device where a product code error correction circuit with comparatively low correction capacity and a humming code error correction circuit are combined, in which correction capacity more than two bit errors without using the error pattern retrieval operation of ROM or the like is realized, and the amount of hardware can be reduced.

CONSTITUTION: In the semiconductor memory device which accumulates information data and parity data, which has a memory array consisting of plural memory cells and plural work lines, which corrects oneself with information data outputted an arbitrary bit line by the selected word line and parity data, a humming encoding/decoding circuit which accumulates information data as holding data, humming code parity data and product code parity data in the memory array, and which individually error - detects parallel or serial output data from the memory array, the product encoding/decoding circuit, and the error correction circuit which refers to detection data of the humming encoding / decoding circuit and the product encoding/decoding circuit, corrects the error and outputs the error to an external part are provided.

?

? t63/9/all

63/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

013873842 **Image available**
WPI Acc No: 2001-358054/200138
XRPX Acc No: N01-260249

Estimation method for relationship between control parameters in digital data compression system, involves estimating adaptive filter parameters in parametric model and providing compensation

Patent Assignee: CANON KK (CANO)
Inventor: NGUYEN E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2795276	A1	20001222	FR 997547	A	19990615	200138 B

Priority Applications (No Type Date): FR 997547 A 19990615

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
FR 2795276	A1	28	H04N-007/50	

Abstract (Basic): FR 2795276 A1

NOVELTY - The method of estimation of a relationship between the control parameters of a system for the **compression** of digital **data** representative of physical quantities and the quantities characterizing the system performance includes an estimation of the parameters of parametric affine model by adaptive filtering. The breakdown of a model is detected by measurement of filter innovations and the detection of variations of the innovations. The model parameters are compensated when the variations are greater than a predetermined threshold. The adaptive filtering is a Recursive Least Square (RLS) filtering. The detection and the compensation are effected by use of the Generalized Likelihood Ratio (GLR).

DETAILED DESCRIPTION - The system quantities include the rate of coded data, and the control parameters are determined for the system providing a predetermined rate or distortion. The system quantities include the distortion of coded data, and the control parameters are determined for the system providing predetermined rate of distortion. A device for an estimation of the relationship between the control parameters and the quantities characterizing the system performance comprises the means for the estimation of parameters of parametric affine model by adaptive filtering, the means for the detection of breakdown of model by measuring the filter innovations and the detection of variations of the innovations, and the means for the compensation of model parameters when the variations are greater than a predetermined threshold. The means for estimation, detection and compensation include a microprocessor, e.g. central processing unit (CPU), a **read - only memory** (ROM) storing a program for signal compression, and a random access **memory** (RAM) containing **data** registers adapted to register the variables modified in the course of program execution. INDEPENDENT CLAIMS are included for an estimation device, and for a digital device comprising the estimation device.

USE - In systems with digital **data compression** , where a control is required to find a compromise between the rate and the distortion; in methods and devices for a robust control of digital **data compression** with losses; for use in systems for video or acoustic

signal processing, in conjunction with digital camera, photographic apparatus, or scanner, or in acoustic case with microphone.

ADVANTAGE - Enables finding the control parameters for the required rate or distortion. The estimation of rate-distortion performance is carried out on line, on the basis of periodically measured values. The system includes a refined stage of model updating.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow chart for an algorithm for digital data compression and estimation of rate-distortion relationship. (Drawing contains non-English language text)

Initialization (E1)
Image reading (E2)
Image compression to given distortion (E3)
Rate measured (E4)
Buffer updating (E5)
Validity test of measured rate (E6)
Model updating (E7)
Distortion determination (E8)
Completeness test (E9)
Integer increased by one (E10)
pp; 28 DwgNo 5/7

Title Terms: ESTIMATE; METHOD; RELATED; CONTROL; PARAMETER; DIGITAL; DATA; COMPRESS; SYSTEM; ESTIMATE; ADAPT; FILTER; PARAMETER; PARAMETER; MODEL; COMPENSATE

Derwent Class: T01; U21; U22; W01; W02; W04

International Patent Class (Main): H04N-007/50

International Patent Class (Additional): H03M-007/30

File Segment: EPI

Manual Codes (EPI/S-X): T01-D02 ; T01-J10D; T01-J18; U21-A05A2; U22-G01A5; W01-A02A ; W01-A07G; W02-C06C; W02-F07; W04-P01A; W04-V05G

63/9/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011986904 **Image available**

WPI Acc No: 1998-403814/199835

XRPX Acc No: N98-314800

Optical memory medium drive unit for CD, CD- ROM , LD - varies
compression rate of data output from optical pick-up which reads
information from optical recording medium

Patent Assignee: ALPINE KK (ALPN)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10162500	A	19980619	JP 96329180	A	19961125	199835 B

Priority Applications (No Type Date): JP 96329180 A 19961125

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10162500	A		10	G11B-020/10	

Abstract (Basic): JP 10162500 A

The optical memory drive unit has an optical pick-up (21) which reads data from CD (100). An error detector detects error from the read data. An optical pick-up drive, returns the pick-up to original position. An encoder (29) compresses the output data from DSP (28) according to rate of data compression sensed by a speed sensor (200).

A DRAM (32) stores the compressed data . A decoder (33) reads data performs expansion of data from the DRAM. Compression is low when the sensor indicates low. When the speed is high, a compression switching device (30) makes the rate of data compression high.

ADVANTAGE - Prevents degraded quality. Provides shock proof.
Increases data storage .

Dwg.1/7

Title Terms: OPTICAL; MEMORY; MEDIUM; DRIVE; UNIT; CD; CD; ROM ; LD; VARY;
COMPRESS; RATE; DATA; OUTPUT; OPTICAL; PICK; UP; READ; INFORMATION;
OPTICAL; RECORD; MEDIUM

Derwent Class: T03; U21; W04

International Patent Class (Main): G11B-020/10

International Patent Class (Additional): G11B-007/00; G11B-019/04;

H03M-007/30

File Segment: EPI

Manual Codes (EPI/S-X): T03-B; T03-F02; T03-P01; U21-A05A2; W04-C;
W04-E02A3

63/9/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011769023 **Image available**

WPI Acc No: 1998-185933/199817

XRPX Acc No: N98-147776

Decoding processing apparatus used in digital data transmission system -
has reading unit which reads decoding data corresponding to received
maximum length encoding data or data error detection
information from ROM

Patent Assignee: NIPPON DENKI ENG KK (NIDE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10041827	A	19980213	JP 96190272	A	19960719	199817 B

Priority Applications (No Type Date): JP 96190272 A 19960719

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 10041827 A 6 H03M-007/16

Abstract (Basic): JP 10041827 A

The apparatus has first flip-flop (2) which latches 4 bit information and encoding data which consists of 11 bit. The signal distance between the encoding data functioning as the data error evaluation standard is stored with decoding data addresses below predetermined threshold value.

A ROM (3) stores the error detection information addresses exceeding the predetermined threshold value. A reading unit reads the decoding data corresponding to the received maximum length encoding data or the data error detection information from the ROM .

ADVANTAGE - Offers hardware failure check function with simple structure.

Dwg.1/8

Title Terms: DECODE; PROCESS; APPARATUS; DIGITAL; DATA; TRANSMISSION;
SYSTEM; READ; UNIT; READ; DECODE; DATA; CORRESPOND; RECEIVE; MAXIMUM;
LENGTH; ENCODE; DATA; DATA; ERROR; DETECT; INFORMATION; ROM

Derwent Class: T03; U21; W01

International Patent Class (Main): H03M-007/16

International Patent Class (Additional): G11B-020/14; G11B-020/18;

H04L-025/08
File Segment: EPI
Manual Codes (EPI/S-X): T03-P01A; U21-A05A2; W01-A01B

63/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011097234 **Image available**
WPI Acc No: 1997-075159/199707
XRPX Acc No: N97-062553

Image data processor e.g. for CD- ROM - has JPEG decoder to perform
expansion of compressed image data per block and obtains expansion
image data

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8321951	A	19961203	JP 95128319	A	19950526	199707 B

Priority Applications (No Type Date): JP 95128319 A 19950526

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8321951	A	15	H04N-001/405	

Abstract (Basic): JP 8321951 A

The processor performs the expansion processing of **compressed image data** and regenerates the **image data** per block. The **compressed image data** is obtained by performing the compression processing of the **image data** corresponding to the pixels forming the image on the screen for every block according to a predetermined rule. A JPEG decoder (11) expands the **compressed image data** per block and outputs an expansion image data 'X(n)'. The number of bits of the expansion image data output from the JPEG decoder is reduced by an error diffusion circuit (12). The error diffusion circuit diffuses the error produced by the reduction of the number of bits to a surrounding pixel.

A **data memory** between blocks (13) delivers a part of the error produced in the error diffusion circuit from the termination of one block to an adjoining block. The **data memory** between blocks is connected to the error diffusion circuit. A lateral image data 'Y(n)' per screen output from the error diffusion circuit is memorised by a pair of **memory areas** (14a,14b) of an image memory (14) alternately. The lateral image data stored in the **memory areas** is read alternately and is boosted to a display processor (15).

ADVANTAGE - Enables to regenerate natural image even when state of screen changes gently. Reduces memory capacity required and thereby reduces cost.

Dwg.1/15

Title Terms: IMAGE; DATA; PROCESSOR; CD; ROM ; DECODE; PERFORMANCE; EXPAND ; COMPRESS; IMAGE; DATA; PER; BLOCK; OBTAIN; EXPAND; IMAGE; DATA

Derwent Class: T01; U21; W02

International Patent Class (Main): H04N-001/405

International Patent Class (Additional): H04N-001/41

File Segment: EPI

Manual Codes (EPI/S-X): T01-J10B1; T01-J10D; U21-A05A2A; W02-J03B2

63/9/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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011093663 **Image available**
WPI Acc No: 1997-071588/199707
XRPX Acc No: N97-059364

Coding-decoding method for digital VTR - involves obtaining coefficient data of AC component whose generation probability is maximum and fed from first memory part of frame decomposition unit

Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8317394	A	19961129	JP 95142581	A	19950517	199707 B

Priority Applications (No Type Date): JP 95142581 A 19950517

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8317394	A	9	H04N-007/30	

Abstract (Basic): JP 8317394 A

The method involves using an ECC circuit (5), whose output signal is fed to a block coding part (21). The coding performs variable length coding of the input data and the error flag which shows the existence of error in variable length information is generated. The data output from a first memory part (22) is fed to ROM (23) and the generation probability of the coefficient data corresponding to the input data, is read-out from the ROM. Then, 256 kinds of generation probabilities are computed by calculation part (24).

The coefficient data whose generation probability is maximum, is selected by a detector (25). The first memory unit, ROM calculation part and the detector, all from port of a first decomposition part (6). The selected data is input into the first memory part and the coefficient data of the AC component whose generation probability is maximum is fed to a block decoding part (7) which perform decoding of that data.

ADVANTAGE - Obtains satisfactory reproduction image, even if error exists in data to be reproduced, by cutting error part of data.

Dwg.7/11

Title Terms: CODE; DECODE; METHOD; DIGITAL; VTR; OBTAIN; COEFFICIENT; DATA; AC; COMPONENT; GENERATE; PROBABILITY; MAXIMUM; FEED; FIRST; MEMORY; PART; FRAME; DECOMPOSE; UNIT

Index Terms/Additional Words: HUFFMAN ; CODING

Derwent Class: U21; W04

International Patent Class (Main): H04N-007/30

International Patent Class (Additional): H03M-007/30 ; H03M-007/40 ; H03M-013/00

File Segment: EPI

Manual Codes (EPI/S-X): U21-A05A2; U21-A05A2A; U21-A06; W04-B10B; W04-B10G; W04-F01F

63/9/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011004723 **Image available**
WPI Acc No: 1996-501673/199650
XRPX Acc No: N96-422988

Analysis device of electrophotographic image forming appts. laser beam

printer - has display which generates warning to user to maintain optical system correctly according to whether peak value is reduced to predetermined level during determination by CPU

Patent Assignee: CANON KK (CANO)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8258330	A	19961008	JP 9564095	A	19950323	199650 B

Priority Applications (No Type Date): JP 9564095 A 19950323

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8258330	A	8	B41J-002/44	

Abstract (Basic): JP 8258330 A

The device has a beam sensor (108) which detects the peak value of a laser beam intensity. An electrically erasable program read only memory (116) stores the obtd. peak value of the intensity of the laser beam during initial coordination. A CPU (114) compares the compare the peak value obtd. during normal use and peak value obtd. during initial coordination. It judges whether the value has reduced

The peak value during the determination by the CPU does not result as a horizontal-synchronising-signal detection error. A display (115) generates a warning to notify the user so that the optical system is regulated early according to the peak value reduced during determination by the CPU.

ADVANTAGE - Detects value of direct intensity of laser beam, or value of intensity of laser beam reflected in polygon mirror. Eliminates state by which horizontal-synchronising-signal detection error is not used.

Dwg.1/3

Title Terms: ANALYSE; DEVICE; ELECTROPHOTOGRAPHIC; IMAGE; FORMING; APPARATUS; LASER; BEAM; PRINT; DISPLAY; GENERATE; WARNING; USER; MAINTAIN ; OPTICAL; SYSTEM; CORRECT; ACCORD; PEAK; VALUE; REDUCE; PREDETERMINED; LEVEL; DETERMINE; CPU

Index Terms/Additional Words: EEPROM

Derwent Class: P75; P84; S06; T04

International Patent Class (Main): B41J-002/44

International Patent Class (Additional): G03G-015/04; G03G-021/00; H04N-001/407

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): S06-A03D; S06-A14B; T04-G04A; T04-G10A

63/9/7 (Item 7 from file: 347)

DIALOG(R)File 347:JAPIO

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03714557 **Image available**
FACSIMILE COMMUNICATION SYSTEM

PUB. NO.: 04-079657 [JP 4079657 A]

PUBLISHED: March 13, 1992 (19920313)

INVENTOR(s): KOIE KOJI

APPLICANT(s): BROTHER IND LTD [000526] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 02-193054 [JP 90193054]

FILED: July 23, 1990 (19900723)

INTL CLASS: [5] H04N-001/00 ; H04N-001/00 ; H04N-001/32 ; H04N-001/41

JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: E, Section No. 1226, Vol. 16, No. 297, Pg. 153, June
30, 1992 (19920630)

ABSTRACT

PURPOSE: To reduce the communication time and communication line using fee by **compressing** each character code **data** constituting a message by means of the same system as that for picture **data** and transmitting the **compressed data** by adding the **compressed data** to **compressed picture data**.

CONSTITUTION: Upon receiving information from a controlling section 11, a CPU 1 **stores** prescribed character selecting **data** **stored** in an EEPROM 24, ROM 23, and RAM 25 in a RAM 26 in accordance with a program stored in the ROM 23. After an **error** correcting code for **detecting** and correcting **errors** is added to the selecting **data** **stored** in the RAM 26 by means of an encoder 113, the character selecting data with the error correcting code are stored in a RAM 112 as N-line picture **data**. The **data** **stored** in the RAM 112 are read out and transmitted after the **data** are **compressed** in the same way as that for picture data by means of the compressing section of a compressing/ extending section 115.

63/9/8 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO
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03195582 **Image available**
FACSIMILE EQUIPMENT

PUB. NO.: 02-171082 [JP 2171082 A]
PUBLISHED: July 02, 1990 (19900702)
INVENTOR(s): SUMITA KAZUYUKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-326847 [JP 88326847]
FILED: December 23, 1988 (19881223)
INTL CLASS: [5] H04N-001/393 ; G06F-003/12; G09G-005/26
JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile); 44.9 (COMMUNICATION --
Other); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: E, Section No. 980, Vol. 14, No. 437, Pg. 148,
September 19, 1990 (19900919)

ABSTRACT

PURPOSE: To generate a character font reduced to 1/2 in the subscanning direction by overwriting a character data onto another data while **deviating** by one **scanning** line in the subscanning direction and thinning the scanning line for an interval of one scanning line from the data.

CONSTITUTION: A CPU 1 reads a designated font data from a font ROM 2 and writes it to a relevant address of a memory 3. Then the CPU 1 deviates the same font data by one scanning line in the subscanning direction while not **deviating** in the main **scanning** direction, and overwrites the **data** onto the **data** **stored** already in the memory 3. At this time, the **data**

of the **memory** 3 becomes to the state shown at the center in a figure. Then the CPU 1 reads out the font **data** from the memory 3, transfers the **data** to a thinning **reduction** processing section 4, in which odd number scanning lines in the subscanning direction are thinned, and its resulting output data is written in the **memory** . Thus, the font **data** is **compressed** to 1/2 in the subscanning direction without missing of dot line elements in the main scanning direction.

63/9/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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02939167 **Image available**
FACSIMILE EQUIPMENT

PUB. NO.: 01-236767 [JP 1236767 A]
PUBLISHED: September 21, 1989 (19890921)
INVENTOR(s): MAEMURA KOICHIRO
TANAKA SHIGETAKA
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-154916 [JP 88154916]
FILED: June 24, 1988 (19880624)
INTL CLASS: [4] H04N-001/32 ; H04L-001/00
JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile); 44.3 (COMMUNICATION --
Telegraphy)
JOURNAL: Section: E, Section No. 861, Vol. 13, No. 568, Pg. 89,
December 15, 1989 (19891215)

ABSTRACT

PURPOSE: To shorten the communication time, to effectively use an ECM, and to simplify an equipment by determining the data transmission speed based on the total number of transmission frames and the number of frames of data error.

CONSTITUTION: A central processing unit CPU 1, a ROM 2, a RAM 3, a scanner 4, a plotter 5, an operation display part 6, a parameter memory 11, an encoding / decoding part 7, a MODEM 8, and a network controller 9 transmit and receive data to and from one another through a bus 10. When the number of times of retransmission of picture information reaches, for example, three, a number (n) of frames of data error is discriminated and the data transmission speed at this time is discriminated. For example, in case of 9600bps, the error rate of the number (n) of frames to a total number N of frames is compared with a set value (a), and the MODEM 8 is controlled to determine 2400bps when the error rate is larger than (a). When it is smaller than (a), the transmission speed is set to 4800bps when it is larger than a set value (b).
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File 348:EUROPEAN PATENTS 1978-2004/May W01

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File 349:PCT FULLTEXT 1979-2002/UB=20040506,UT=20040429

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Set	Items	Description
S1	363	JEDEC OR (JT OR JOINT)()ELECTRONIC?? ?()DEVICE? ? ()ENGINE- ER? ? OR JESD3()C OR JESD()3
S2	40877	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPL- DS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FGAS
S3	172165	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR- OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S4	156981	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S5	3738	S4(1W)LOGIC(1W)DEVICE? ?
S6	3106	S4(1W)LOGIC(1N)ARRAY? ?
S7	4883	S4(1W)GATE? ?(1W)ARRAY? ?
S8	97	S4()(IC OR ICS)
S9	545	S4(1W)INTEGRATED()CIRCUIT???? ?
S10	0	S4(1W)ELLECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S11	73	GENERIC(1W)ARRAY? ?(1W)LOGIC? ?
S12	39255	(READONLY OR READ()ONLY)(1W)(MEMORY? OR MEMORIES OR STORAG- E?)
S13	607469	STORAGE? OR STORE? ? OR STORING OR MEMORY? OR MEMORIES OR - PRESTOR??? ?
S14	112744	S13(3N)(FIELD? ? OR SPACE? ? OR AREA? ? OR REGION? ? OR SE- CTOR? ? OR ZONE? ? OR SECTION? ? OR PART OR PARTS OR PORTION? ?)
S15	157762	S13(3N)DATA
S16	88188	S13(3N)(PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PRO- PERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATT- RIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR - FEATURES)
S17	0	S4(1W)ELECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S18	4848	BINARY(1W)TREE? ? OR HUFFMAN
S19	1193205	PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PROPERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATTRIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR FEATURES
S20	84201	S19(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACK- ED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDU- C? OR REDN? ? OR DIMINISH?)
S21	95538	S19(3N)(REDUC??? ? OR REDUCTION? OR DECREAS? OR DECREMENT? OR ENCOD??? ? OR CODIFY? OR CODIFIE? OR CODIFIC? OR INCOD??? - ?)
S22	400787	NONCONFORM? OR INCOMPAT? OR INOPERA? OR UNUSUAL OR DYSFUNC- T? OR INCOMPLETE? OR DEVIA? OR IRREGULAR? OR EXCEPTION? ? OR - DISTORT?
S23	375134	DISFUNCT? OR UNCONFORM? OR UNCOMPAT? OR UNCOMPLET? OR DISC- REPAN? OR DEGRAD? OR DISPARAT? OR BUG? ? OR ERROR? ? OR CORRUP- T? OR INVALID?
S24	990838	MISTAK? OR FAIL???? ? OR PROBLEM? ? OR FAULT? OR DEFECT? OR DEFICIEN? OR ABNORMA? OR DAMAG? OR FLAW? OR IMPAIR?
S25	68983	ABERRA? OR MALFUNCTI? OR IMPERFECT?
S26	12449	DEBUG? OR DE()BUG???? ? OR ECC OR ECCS OR EDAC OR EDACS
S27	21	S4(1W)ELECTRICAL?? ?(1W)ERAS(1W)LOGIC? ?
S28	119531	S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH- EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PRO- BING? OR SEARCH? OR SURVEY?)
S29	43195	S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? -

OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR
LOCAT? OR REVIEW?)

S30 76373 S22:S25(3N)(DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENT-
IFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECO-
GNIS? OR RECOGNIZ? OR RECOGNIT?)

S31 123289 S22:S25(3N)(INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR
SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT???
? OR FILTER??? ?)

S32 37 (S2:S3 OR S5:S12 OR S27)(25N)S1

S33 31266 (S2:S3 OR S5:S12 OR S27)(25N)S14:S16

S34 178 S33(25N)(S18 OR S20:S21)

S35 45877 DATA(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PAC-
KED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR RED-
UC? OR REDN? ? OR DIMINISH?)

S36 32684 DATA(3N)(DECREAS? OR DECREMENT? OR ENCOD???? ? OR CODIFY? -
OR CODIFIE? OR CODIFIC? OR INCOD??? ?)

S37 903 S33(25N)S35:S36

S38 0 (S34 OR S37)(25N)S1

S39 16 (S34 OR S37)(25N)S26

S40 119531 S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH-
EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PRO-
BING? OR SEARCH? OR SURVEY?)

S41 43195 S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? -
OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR
LOCAT? OR REVIEW?)

S42 76373 S22:S25(3N)(DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENT-
IFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECO-
GNIS? OR RECOGNIZ? OR RECOGNIT?)

S43 123289 S22:S25(3N)(INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR
SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT???
? OR FILTER??? ?)

S44 23 (S34 OR S37)(25N)S40:S43

S45 32 S39 OR S44

S46 32 IDPAT (sorted in duplicate/non-duplicate order)

S47 31 IDPAT (primary/non-duplicate records only)

? t47/5,k/9,11,13-16

47/5,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01113164

Disk recording system

Plattenaufzeichnungssystem

Système d'enregistrement de disque

PATENT ASSIGNEE:

Sanyo Electric Co., Ltd., (2206450), 5-5, Keihanondori 2-chome,
Moriguchi-shi, Osaka, (JP), (Proprietor designated states: all)

INVENTOR:

Tsukihashi, Akira, 1314-11, Yorikido, Ohizumi-machi, Ohra-gun, Gunma,
(JP)

LEGAL REPRESENTATIVE:

Cross, Rupert Edward Blount et al (42891), BOULT WADE TENNANT, Verulam
Gardens 70 Gray's Inn Road, London WC1X 8BT, (GB)

PATENT (CC, No, Kind, Date): EP 974966 A1 000126 (Basic)
EP 974966 B1 031022

APPLICATION (CC, No, Date): EP 99305602 990715;

PRIORITY (CC, No, Date): JP 98206548 980722

DESIGNATED STATES: DE; ES; FR; GB; IT; NL

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G11B-020/10; G11B-019/02

CITED PATENTS (EP B): EP 520381 A; EP 726571 A; EP 825602 A; US 5315571 A;
US 5343455 A; US 5583838 A

CITED REFERENCES (EP B):

PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10, 31 October 1996 (1996-10-31)
& JP 08 147879 A (YAMAHA CORP), 7 June 1996 (1996-06-07);

ABSTRACT EP 974966 A1

When a buffer underrun decision circuit (17) decides that a buffer underrun is about to occur, data recording on the disk is interrupted by a recording control circuit (18). On the other hand, when the buffer underrun decision circuit (17) determines that a buffer underrun situation has been avoided, data recording is resumed by the recording control circuit (18). At this time, data recording is resumed from a position of the disk which is continuous to data recorded by the time the data recording was interrupted, thereby recording new data continuous to the last recorded data.

ABSTRACT WORD COUNT: 97

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant: 031022 B1 Granted patent

Application: 20000126 A1 Published application with search report

Examination: 20000426 A1 Date of request for examination: 20000228

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200004	575
CLAIMS B	(English)	200343	579
CLAIMS B	(German)	200343	501
CLAIMS B	(French)	200343	708
SPEC A	(English)	200004	3837
SPEC B	(English)	200343	3793
Total word count - document A			4413

Total word count - document B 5581
Total word count - documents A + B 9994

...SPECIFICATION and from a host personal computer 10 connected outside the system. Numeral 11 denotes an **encoder** which modulates **data** input thereto via the interface 8 into recording data to be recorded in the disk and 12 denotes an input **data** RAM for **storing** input **data** to be modulated by the encoder 11.

When the **encoder** 11 modulates **data** based on the CD- ROM standard, a sync, a header, an EDC (**Error Detection Code**), and an ECC (Error Correction Code) for CD-ROM data are added to the input data. Subsequently, a...

...SPECIFICATION and from a host personal computer 10 connected outside the system. Numeral 11 denotes an **encoder** which modulates **data** input thereto via the interface 8 into recording data to be recorded in the disk and 12 denotes an input **data** RAM for **storing** input **data** to be modulated by the encoder 11.

When the **encoder** 11 modulates **data** based on the CD- ROM standard, a sync, a header, an EDC (**Error Detection Code**), and an ECC (Error Correction Code) for CD-ROM data are added to the input data. Subsequently, a...

47/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00765243

METHOD FOR RECORDING/REPRODUCING DATA, DATA REPRODUCING DEVICE, AND RECORDING MEDIUM

DATENAUFZEICHNUNGS-/WIEDERGABEVERFAHREN, DATENWIEDERGABEVORRICHTUNG, UND AUFZEICHNUNGSMEDIUM

PROCEDE D'ENREGISTREMENT/DE RESTITUTION DE DONNEES, DISPOSITIF DE RESTITUTION DE DONNEES ET SUPPORT D'ENREGISTREMENT

PATENT ASSIGNEE:

SONY CORPORATION, (214021), 7-35 Kitashinagawa 6-chome Shinagawa-ku,
Tokyo 141, (JP), (Proprietor designated states: all)

INVENTOR:

SAKO, Yoichiro, Sony Corporation 7-35, Kitashinagawa 6-chome,
Shinagawa-ku Tokyo 141, (JP)
YAMAGAMI, Tamotsu, Sony Corporation 7-35, Kitashinagawa 6-chome,
Shinagawa-ku Tokyo 141, (JP)
OTSUKA, Satoshi, Sony Corporation 7-35, Kitashinagawa 6-chome,
Shinagawa-ku Tokyo 141, (JP)
TOBITA, Minoru, Sony Corporation 7-35, Kitashinagawa 6-chome,
Shinagawa-ku Tokyo 141, (JP)

LEGAL REPRESENTATIVE:

Melzer, Wolfgang, Dipl.-Ing. et al (8278), Patentanwalte Mitscherlich &
Partner, Sonnenstrasse 33, 80331 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 729150 A1 960828 (Basic)
EP 729150 A1 980520
EP 729150 B1 031203
WO 96008010 960314

APPLICATION (CC, No, Date): EP 95930703 950906; WO 95JP1766 950906

PRIORITY (CC, No, Date): JP 94216315 940909

DESIGNATED STATES: DE; FR; GB; NL

INTERNATIONAL PATENT CLASS: G11B-020/12

CITED PATENTS (EP B): JP 3122870 A; JP 4139664 A; JP 4159661 A; JP 55004774
A; JP 62271535 A; JP 63157374 A; JP 63253573 A; US 4680764 A

CITED PATENTS (WO A): US 267723 A ; US 5304359 A ; WO 8200478 A

CITED REFERENCES (EP B):

PATENT ABSTRACTS OF JAPAN vol. 16, no. 454 (P-1425), 21 September 1992 &
JP 04 159661 A (OLYMPUS OPTICAL CO LTD), 2 June 1992,;

ABSTRACT EP 729150 A1

Data recorded on such a recording medium as an optical disk, are reproduced excellently even when burst errors occur during reproduction, without reducing the data record capacity of the recording medium. A first error correcting code is generated for every block of a certain amount of data, and added to the corresponding block, a second error correcting code is generated for the every block and added to the other blocks than the block for which the second error correcting code is generated. These data and codes are recorded on the recording medium. When reproducing the data, recorded on the recording medium in blocks of data, whether or not detection correction is possible or not is judged based on the first error correcting codes included in the reproduced data. When the detection correction of a block is possible, the detection correction is performed, and when impossible, missing information is generated based on the second error correcting codes reproduced from the data blocks and corresponding to the block of which detection correction is impossible. Using the missing information and the first error correcting code, missing correction of the data block is performed. (see image in original document)

ABSTRACT WORD COUNT: 21487

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant: 031203 B1 Granted patent
Application: 960619 A International application (Art. 158(1))
Application: 960828 A1 Published application (A1with Search Report
;A2without Search Report)
Examination: 960828 A1 Date of filing of request for examination:
960419
Search Report: 980520 A1 Drawing up of a supplementary European search
report: 980403
Examination: 981014 A1 Date of despatch of first examination report:
980828

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	2018
CLAIMS B	(English)	200349	2415
CLAIMS B	(German)	200349	2254
CLAIMS B	(French)	200349	2856
SPEC A	(English)	EPAB96	18113
SPEC B	(English)	200349	17353
Total word count - document A			20135
Total word count - document B			24878
Total word count - documents A + B			45013

...SPECIFICATION mode stored therein, a RAM 63 used as a work area such as the program data stored in the ROM 62, an input/output port 64, a decoder 67 for error -correcting and error - checking reproduced data , an encoder 68 for generating a parity-check code for data supplied thereto from the host computer...

...SPECIFICATION shown in FIG. 2.

In the controller 44 shown in FIG. 3, a bus 61 composed of an address bus , a data bus and a control bus is connected to a CPU

(central processing unit) 60. A ROM 62 with various program data and parameter data for effecting processing in the reproducing operation mode stored therein, a RAM 63 used as a work area such as the program data stored in the ROM 62, an input/output port 64, a decoder 67 for error-correcting and error-checking reproduced data, an encoder 68 for generating a parity-check code for data supplied thereto from the host computer...

47/5,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00760823

Image processing and recording media
Bildverarbeitung und Aufzeichnungsträger
Traitement d'image et moyen d'enregistrement

PATENT ASSIGNEE:

SONY CORPORATION, (214024), 6-7-35 Kitashinagawa Shinagawa-ku, Tokyo, (JP), (applicant designated states: AT;CH;GB;IT;LI;SE)

INVENTOR:

Tanaka, Masayoshi, c/o Intellectual Prop. Div., Sony Corp., 7-6-35 Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP)
Suzuoki, Masakazu, c/o Intellectual Prop. Div., Sony Corp., 7-6-35 Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP)
Okada, Toyoshi, c/o Intellectual Prop. Div., Sony Corp., 7-6-35 Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP)

LEGAL REPRESENTATIVE:

Cotter, Ivan John et al (29661), D. YOUNG & CO. 21 New Fetter Lane, London EC4A 1DA, (GB)

PATENT (CC, No, Kind, Date): EP 715279 A2 960605 (Basic)
EP 715279 A3 970226

APPLICATION (CC, No, Date): EP 95308662 951201;

PRIORITY (CC, No, Date): JP 94300029 941202

DESIGNATED STATES: AT; CH; GB; IT; LI; SE

INTERNATIONAL PATENT CLASS: G06T-015/10;

ABSTRACT EP 715279 A2

An image data processing system includes a geometry transfer engine (GTE) (61) and a graphic processing unit (GPU) (62) which act in combination as a transforming means for converting three-dimensional image data retrieved from a CD-ROM disk (81) into two-dimensional image data for drawing an image on a two-dimensional display screen, and a frame buffer (63) which serves as a memory having an image data storage area (picture data area) for storage of the image data and at least a color data tables storage area (CLUT area) for storage of multiple color lookup data tables in a two-dimensional arrangement, each color data table including a color data wherein the structure is arranged substantially identical to that of each pixel of data in the image. A greater number of colors are thus facilitated and the data processing is simplified. (see image in original document)

ABSTRACT WORD COUNT: 165

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee: 001227 A2 Transfer of rights to new applicant: Sony Computer Entertainment Inc. (3064090) 7-1-1 Akasaka, Minato-ku Tokyo 107-0052 JP
Application: 960605 A2 Published application (Alwith Search Report ;A2without Search Report)
Change: 031001 A2 Title of invention (German) changed: 20030813
Examination: 010530 A2 Date of dispatch of the first examination

report: 20010412
Search Report: 970226 A3 Separate publication of the European or
International search report
Examination: 970910 A2 Date of filing of request for examination:
970711

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	510
SPEC A	(English)	EPAB96	7223
Total word count - document A			7733
Total word count - document B			0
Total word count - documents A + B			7733

...SPECIFICATION disk drive 81 for retrieving a program or data from an optical disk of CD- ROM , a decoder 82 for decoding an encoded , stored program or data accompanied with error correction codes (ECC), and a buffer 83 of, for example, 32 kilobytes for storage of data retrieved from...

47/5,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00760561

Method of producing image data and associated recording medium
Verfahren zur Erzeugung von Bilddaten und zugehöriger Aufzeichnungsträger
Methode pour produire des donnees d'image et support d'enregistrement
associe

PATENT ASSIGNEE:

Sony Computer Entertainment Inc., (3064090), 7-1-1 Akasaka, Minato-ku,
Tokyo 107-0052, (JP), (Proprietor designated states: all)

INVENTOR:

Suzuoki, Masakazu, c/o SONY CORP, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)
Furuhashi, Makoto, c/o SONY CORP, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)
Tanaka, Masayoshi, c/o SONY CORP, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)
Yutaka, Teiji, c/o SONY CORP, 7-35, Kitashinagawa 6-chome, Shinagawa-ku,
Tokyo, (JP)

LEGAL REPRESENTATIVE:

Muller, Frithjof E., Dipl.-Ing. et al (8661), Muller Hoffmann & Partner
Patentanwalte Innere Wiener Strasse 17, 81667 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 715278 A2 960605 (Basic)
EP 715278 A3 960710
EP 715278 B1 021023

APPLICATION (CC, No, Date): EP 95118965 951201;

PRIORITY (CC, No, Date): JP 94300021 941202

DESIGNATED STATES: AT; DE; DK; ES; GB

INTERNATIONAL PATENT CLASS: G06T-015/10; G06T-015/50

CITED PATENTS (EP B): GB 2272137 A

ABSTRACT EP 715278 A3

A data format is provided capable of assigning a desired color lookup table (CLUT) to a texture pattern of each polygon drawn on a two-dimensional display screen. Assuming that TPF represents a pixel depth of the texture pattern, when TPF is 00, 01, and 10, the format (CLUT) is applied of a 4-bit mode, an 8-bit mode, and 16-bit mode respectively, whereby its related command is decreased in word length

and thus requires less storage in a source video memory. (see image in original document)
ABSTRACT WORD COUNT: 101
NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination: 001018 A2 Date of dispatch of the first examination report: 20000905
Application: 960605 A2 Published application (A1with Search Report ;A2without Search Report)
Lapse: 040121 B1 Date of lapse of European Patent in a contracting state (Country, date): AT 20021023, ES 20030429,
Lapse: 030910 B1 Date of lapse of European Patent in a contracting state (Country, date): AT 20021023,
Assignee: 001025 A2 Transfer of rights to new applicant: Sony Computer Entertainment Inc. (3064090) 7-1-1 Akasaka, Minato-ku Tokyo 107-0052 JP
Grant: 021023 B1 Granted patent
Oppn None: 031015 B1 No opposition filed: 20030724
Change: 960703 A2 Obligatory supplementary classification (change)
Search Report: 960710 A3 Separate publication of the European or International search report
Examination: 970212 A2 Date of filing of request for examination: 961211
Change: 970319 A2 Representative (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1356
CLAIMS B	(English)	200243	621
CLAIMS B	(German)	200243	555
CLAIMS B	(French)	200243	756
SPEC A	(English)	EPAB96	9584
SPEC B	(English)	200243	9482
Total word count - document A			10943
Total word count - document B			11414
Total word count - documents A + B			22357

...SPECIFICATION disk drive 81 for retrieving a program or data from an optical disk of CD- ROM , a decoder 82 for decoding an encoded , stored program or data accompanied with error correction codes (ECC), and a buffer 83 of, for example, 32 kilobytes for storage of data retrieved from...

...SPECIFICATION disk drive 81 for retrieving a program or data from an optical disk of CD- ROM , a decoder 82 for decoding an encoded , stored program or data accompanied with error correction codes (ECC), and a buffer 83 of, for example, 32 kilobytes for storage of data retrieved from...

47/5,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00760369

Method of producing image data, image data processing apparatus, and

recording medium

Bilddatenerzeugungsverfahren, Bilddatenverarbeitungsgerät und Aufzeichnungsmedium

Methode pour produire des donnees d'image, appareil de traitement de donnees d'image et support d'enregistrement

PATENT ASSIGNEE:

SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo, (JP), (applicant designated states: AT;BE;DE;FR;GB;NL)

INVENTOR:

Tanaka, Masayoshi, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)

Oka, Masaaki, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)

Yutaka, Teiji, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)

Hagiwara, Kaoru, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)

Ichioka, Hidetoshi, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)

LEGAL REPRESENTATIVE:

Muller, Frithjof E., Dipl.-Ing. et al (8661), Patentanwalte MULLER & HOFFMANN, Innere Wiener Strasse 17, 81667 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 715277 A2 960605 (Basic)

EP 715277 A3 960821

APPLICATION (CC, No, Date): EP 95118239 951120;

PRIORITY (CC, No, Date): JP 94300020 941202

DESIGNATED STATES: AT; BE; DE; FR; GB; NL

INTERNATIONAL PATENT CLASS: G06T-015/10; G06T-017/00;

ABSTRACT EP 715277 A3

A method and apparatus includes a geometry transfer engine (GTE) 61 acting as a coordinate transforming means for converting three-dimensional image data of TMD format into two-dimensional image data by perspective view transformation, and a graphics processing unit (GPU) 62 acting as a drawing means for transferring the two-dimensional image data in a given transmission standard to draw an image on a two-dimensional display screen. A structure of the three-dimensional image data, excluding the information to be perspective view transformed, is arranged identical to that of the given transmission standard of the two-dimensional image data. Accordingly, in the GTE 61, the information to be perspective view transformed is discriminated from the other data of the three-dimensional image data wherein the structure is identical to that of the given transmission standard of the two-dimensional image data, subjected to the perspective view transformation, and is combined with the other data wherein the structure is identical to that of the given transmission standard for production of the two-dimensional image data. An original format file including data to be transformed is thereby easily converted into a file having a new format. (see image in original document)

ABSTRACT WORD COUNT: 222

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination: 001018 A2 Date of dispatch of the first examination report: 20000905

Application: 960605 A2 Published application (A1with Search Report ;A2without Search Report)

Assignee: 001025 A2 Transfer of rights to new applicant: Sony Computer Entertainment Inc. (3064090) 7-1-1 Akasaka, Minato-ku Tokyo 107-0052 JP

Change: 960814 A2 Obligatory supplementary classification (change)

Search Report: 960821 A3 Separate publication of the European or
International search report
Change: 970319 A2 Representative (change)
Examination: 970326 A2 Date of filing of request for examination:
970122

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1187
SPEC A	(English)	EPAB96	12151
Total word count - document A			13338
Total word count - document B			0
Total word count - documents A + B			13338

...SPECIFICATION disk drive 81 for retrieving a program or data from an
optical disk of CD- ROM , a decoder 82 for decoding an encoded ,
stored program or data accompanied with error correction codes (ECC
) , and a buffer 83 of, for example, 32 kilobytes for storage of data
retrieved from...

47/5,K/16 (Item 16 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00753610

Method of and apparatus for recording and reproducing data and transmitting
data

Verfahren und Vorrichtung zur Datenaufzeichnung und Wiedergabe und
Datenubertragung

Methode et appareil pour l'enregistrement et la reproduction de donnees et
la transmission de donnees

PATENT ASSIGNEE:

SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku,
Tokyo, (JP), (Proprietor designated states: all)

INVENTOR:

Sako, Yoichiro, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)

Otsuka, Satoshi, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)

Yamagami, Tamotsu, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, (JP)

LEGAL REPRESENTATIVE:

Melzer, Wolfgang, Dipl.-Ing. et al (8278), Patentanwalte Mitscherlich &
Partner, Sonnenstrasse 33, 80331 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 709846 A2 960501 (Basic)
EP 709846 A3 980311
EP 709846 B1 010926

APPLICATION (CC, No, Date): EP 95116741 951024;

PRIORITY (CC, No, Date): JP 94258522 941024

DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: G11B-020/18

CITED PATENTS (EP B): US 4680764 A; US 4802169 A; US 5272692 A

CITED REFERENCES (EP B):

E. FUJIWARA ET AL.: "Cross-Interleave Reed-Solomon Code" ESSENTIALS OF
ERROR-CONTROL CODING TECHNIQUES, 1990, pages 237-245, XP002048536;

ABSTRACT EP 709846 A2

First error-processing data are generated (39) with respect to a
predetermined amount of data, and second error-processing data are

generated (40) with respect to each of a plurality of blocks produced by dividing the predetermined amount of data. Data of record units are generated from the predetermined amount of data, the first error-processing data, and the second error-processing data. The data of record units are recorded (8) on and reproduced from a recording medium (4). Errors are corrected (2) in the predetermined amount of data in the reproduced data of record units with the first error-processing data with respect to each of the record units. If errors cannot be corrected, at least errors are detected in the predetermined amount of data in each of the blocks with the second error-processing data. If errors are detected in N (N is a positive integer) successive blocks, all data in at least one block which is not positioned at an end of the N successive blocks are regarded as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data, thus producing reproduced data. (see image in original document)

ABSTRACT WORD COUNT: 222

NOTE:

Figure number on first page: 3

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant: 010926 B1 Granted patent
 Application: 960501 A2 Published application (Alwith Search Report ;A2without Search Report)
 Oppn None: 020918 B1 No opposition filed: 20020627
 Search Report: 980311 A3 Separate publication of the European or International search report
 Examination: 980909 A2 Date of filing of request for examination: 980714
 Examination: 981014 A2 Date of despatch of first examination report: 980828

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	2828
CLAIMS B	(English)	200139	1128
CLAIMS B	(German)	200139	1039
CLAIMS B	(French)	200139	1312
SPEC A	(English)	EPAB96	14873
SPEC B	(English)	200139	13230
Total word count - document A			17705
Total word count - document B			16709
Total word count - documents A + B			34414

...SPECIFICATION 60 and composed of an address bus, a data bus, and a control bus, a ROM 62 for storing various program data, parameter data, etc. for effecting various processes in the reproducing mode, a RAM 63 for use as a work storage area for storing program data, parameter data, etc. which are stored in the ROM 62, and an input/output port 64. The controller 44 also has a decoder 67 for effecting error correction and error checking on reproduced data, an encoder 68 for generating parity data with respect to data supplied from the host computer 3...

...SPECIFICATION 60 and composed of an address bus, a data bus, and a control bus, a ROM 62 for storing various program data, parameter data, etc. for effecting various processes in the reproducing mode, a RAM 63 for use as a work storage area for storing program data, parameter data, etc. which are stored in the ROM 62, and an input/output port 64. The controller 44 also has a decoder 67 for

effecting error correction and error **checking** on reproduced **data** , an **encoder** 68 for generating parity data with respect to data supplied from the host computer 3...

? t47/5,k/19,23,29

47/5,K/19 (Item 19 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00567031

Memory card device

Speicherkartengerat

Dispositif de carte a memoire

PATENT ASSIGNEE:

KABUSHIKI KAISHA TOSHIBA, (213130), 72, Horikawa-cho, Saiwai-ku,
Kawasaki-shi, Kanagawa-ken 210-8572, (JP), (applicant designated
states: DE;FR;GB)
TOSHIBA AVE CO., LTD, (722723), 3-3-9, Shinbashi, Minato-ku, Tokyo 105,
(JP), (applicant designated states: DE;FR;GB)

INVENTOR:

Konishi, Kazuo, c/o Int. Property Division, Kabushiki Kaisha Toshiba, 1-1
Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)
Yoshioka, Shimpei, c/o Int. Property Division, Kabushiki Kaisha Toshiba,
1-1 Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)
Maruyama, Koji, c/o Int. Property Division, Kabushiki Kaisha Toshiba, 1-1
Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)
Maekawa, Tomoyuki, c/o Int. Property Division, Kabushiki Kaisha Toshiba,
1-1 Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)
Sato, Toshiaki, c/o Int. Property Division, Kabushiki Kaisha Toshiba, 1-1
Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)

LEGAL REPRESENTATIVE:

Henkel, Feiler, Hanzel (100401), Mohlstrasse 37, 81675 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 569040 A2 931110 (Basic)
EP 569040 A3 950308
EP 569040 B1 990728

APPLICATION (CC, No, Date): EP 93107569 930510;

PRIORITY (CC, No, Date): JP 11563092 920508; JP 11601892 920508

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-011/20; G06F-011/00;

ABSTRACT EP 569040 A2

This invention provides a memory card device using an EEPROM (16) as a semiconductor memory. When a data write-in defective area is detected in the storage area of the EEPROM (16), a space area is retrieved from the storage area of the EEPROM (16) as a relieving area and data to be written into the data write-in defective area is written into the relieving area. Then, when the relieving area becomes full and a data write-in defective area is detected in the storage area of the EEPROM (16), another space area is retrieved from the storage area of the EEPROM (16) as a new relieving area and data to be written into the data write-in defective area is written into the new relieving area. (see image in original document)

ABSTRACT WORD COUNT: 131

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None: 000712 B1 No opposition filed: 20000429
Application: 931110 A2 Published application (Alwith Search Report
;A2without Search Report)
Examination: 931110 A2 Date of filing of request for examination:
930607
Change: 950222 A2 Obligatory supplementary classification
(change)
Search Report: 950308 A3 Separate publication of the European or

International search report

Examination: 980401 A2 Date of despatch of first examination report:
980216

Grant: 990728 B1 Granted patent

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9930	743
CLAIMS B	(German)	9930	637
CLAIMS B	(French)	9930	866
SPEC B	(English)	9930	5773
Total word count - document A			0
Total word count - document B			8019
Total word count - documents A + B			8019

...CLAIMS indicating attribute information of data written into the block
is stored is provided in the **storage area** of said EEPROM (16) and
the remaining storage capacity of the **storage area** of said
EEPROM (16) into which data can be written is written into the
attribute area .

10. The **memory** card device according to claim 9

whereby the remaining storage capacity written into the **attribute**
area is **reduced** according to the capacity of the data write-in
defective area and the capacity of the data relieving area when the
data write-in **defective** area is **detected** in the storage area of
said EEPROM (16) by said relieving means and data to...

47/5,K/23 (Item 23 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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01109996 **Image available**

IMAGE DISPLAY SYSTEM

SYSTEME AFFICHEUR D'IMAGE

Patent Applicant/Assignee:

PIXIA CORP, 21025 Stanford Square, Suite 401, Sterling, VA 20166, US, US
(Residence), US (Nationality), (For all designated states except: US)

Patent Applicant/Inventor:

ERNST Rudolf O, 800 Lake Park Drive, Union Hall, VA 24176, US, US
(Residence), CH (Nationality), (Designated only for: US)

LUI Pun Sing, RM 1903 Harbor Centre, Hong Kong, HK, CN (Residence), CN
(Nationality), (Designated only for: US)

Legal Representative:

MOORE Steven (agent), 1600 Tysons Boulevard, McLean, VA 22102, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200432107 A2 20040415 (WO 0432107)

Application: WO 2003US30639 20030930 (PCT/WO US03030639)

Priority Application: US 2002263930 20021003

Parent Application/Grant:

Related by Continuation to: US 2002263930 20021003 (CIP)

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO

RU SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE
SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G09G
Publication Language: English
Filing Language: English
Fulltext Availability:
 Detailed Description
 Claims
Fulltext Word Count: 11233

English Abstract

An image display system is disclosed that enables users to navigate very large digital images quickly and seamlessly. The system is optimized to transmit image data from a disk drive to a display at high data rates. The image data is stored on the disk drive in a file format optimized for high speed retrieval, display, and seamless navigation. The image display system can be cascaded for showing two or more contiguous images on multiple displays.

French Abstract

La presente invention concerne un systeme afficheur d'image qui permet a des utilisateurs de naviguer dans de tres grandes images numeriques rapidement et en continu. Ce systeme est optimise pour transmettre des donnees image d'un lecteur de disque a un afficheur a hauts debits de donnees. Les donnees image sont stockees sur un lecteur de disque dans un format de fichier optimise en vue d'une localisation, d'un affichage et d'une navigation en continu a vitesse elevee. Ce systeme afficheur d'image peut etre monte en cascade de maniere a montrer au moins deux images contigues sur des afficheurs multiples.

Legal Status (Type, Date, Text)

Publication 20040415 A2 Without international search report and to be republished upon receipt of that report.

Fulltext Availability:
 Detailed Description

Detailed Description

... use of USB ports for providing improved communication with the system such as for acquiring **debugging** messages. A further advantage is the use of a more sophisticated **FPGA** allowing for real-time manipulation of data. For example, image **data** can be **stored compressed** on the disk 10 drive and then decompressed in real time using the **FPGA** when the data is needed for viewing.

[00040] The software embodiment of the present invention...

47/5,K/29 (Item 29 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00272765

MULTI-MODE IDENTIFICATION SYSTEM SYSTEME D'IDENTIFICATION MULTI-MODE

Patent Applicant/Assignee:

AVID MARKETING INC,
BEIGEL Michael L,
POLISH Nathaniel,
MALM Robert E,

Inventor(s):

BEIGEL Michael L,
POLISH Nathaniel,
MALM Robert E,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9420941 A1 19940915
Application: WO 93US2112 19930310 (PCT/WO US9302112)
Priority Application: WO 93US2112 19930310

Designated States: AT AU BB BG BR CA CH CZ DE DK ES FI GB HU JP KP KR KZ LK
LU MG MN MW NL NO NZ PL PT RO RU SD SE SK UA US VN AT BE CH DE DK ES FR
GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR SN TD TG

Main International Patent Class: G08C-019/06

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 12519

English Abstract

A multi-mode identification system is comprised of readers and tags wherein a reader (100) in the proximity of and inductively coupled (100) to a tag (200) interrogates and obtains a response from the tag (200) in accordance with a specified process if the tag (200) belongs to a certain class of tags. The response consists of an identification code unique to the tag (200) together with the data supplied by sensors (270, 275) incorporated within the tag (200). Communication between tag (200) and reader (100) is accomplished by a reader (100) establishing a reversing magnetic field in the vicinity of a tag (200) and the tag (200) varying its absorption of power from the field in accordance with the information to be transmitted. The reader (100) detects these variations in power absorption and extracts from these variations the information transmitted by the tag (200).

French Abstract

Un systeme d'identification multi-mode est compose de "lecteurs" et "d'etiquettes". Dans ce systeme, un lecteur (100) a proximite d'une etiquette (200) et couple inductivement (100) a cette etiquette, interroge et obtient une reponse de l'etiquette (200) correspondant avec un traitement specifique si l'etiquette appartient a une certaine classe d'etiquettes. La reponse consiste en un code d'identification particulier a l'etiquette (200) avec des donnees fournies par des detecteurs (270, 275) incorpores dans l'etiquette (200). La communication entre l'etiquette (200) et le lecteur (100) est etablie par un lecteur (100) creant un champ magnetique s'inversant a proximite d'une etiquette (200), l'etiquette (200) modifiant son absorption de puissance du champ selon les informations a transmettre. Le lecteur (100) detecte ces variations d'absorption de puissance et retire de ces variations les informations transmises par l'etiquette (200).

Fulltext Availability:

Detailed Description

Detailed Description

... for one type of

tag or for a variety of tags by means of "model" data stored in read - only memory in the form of an integrated circuit, a resistor matrix, or any other means for permanently storing 35 binary data. Mode data include driving frequency, type of modulation (i.e, FSKj, OOK, CPSK, and DCPSK), "mark" and "space" frequencies,, bit rate, data encoding if any (e,g, PCT[US93/02112 Manchester or related coding techniques) "start message"

code, error detection process (e.g. cyclic redundancy checks, parity checks), tag type, and all of the constants...
? t47/5,k/31

47/5,K/31 (Item 31 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00236272

**METHOD AND APPARATUS FOR DETECTING AND CORRECTING ERRORS IN DATA ON
MAGNETIC TAPE MEDIA**

**PROCEDE ET APPAREIL DE DETECTION ET DE CORRECTION D'ERREURS DANS DES
DONNEES ENREGISTREES SUR SUPPORT MAGNETIQUE**

Patent Applicant/Assignee:

STORAGE TECHNOLOGY CORPORATION,

Inventor(s):

DODT William Carl,
LIEHE Thomas Gardiner,
McCARTHY Donald Francis,
MILLIGAN Charles Allen,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9310534 A1 19930527

Application: WO 92US9598 19921112 (PCT/WO US9209598)

Priority Application: US 91791793 19911112

Designated States: AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE

Main International Patent Class: G11B-020/18

International Patent Class: H03M-13:00; G11B-20:12

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 10876

English Abstract

The helical scan data write circuits (410, 321) operate on the received stream of data records to produce two orthogonal error detection and correction codes on a scan group level. The data write circuit (410, 321) divides the received stream of data records into data segments, each of which contains a predetermined number of data bytes. A first of these scan group error codes is generated on a per data segment basis while a second scan group error code is generated across multiple data segments. A third level error correcting code (ECC-3) is also used to protect an entire scan group (700) rather than data on a per byte basis. The third level error correction code generator (805) produces an error code over a predetermined number of sequentially written scan groups (700) to enable the control unit (350) to reconstruct an entire scan group (700) if its data integrity is comprised.

French Abstract

Les circuits (410, 321) d'écriture de données à balayage hélicoïdal agissent sur le flux reçu de données enregistrées afin de produire deux codes orthogonaux de détection et de correction d'erreurs sur un niveau de groupe de défilement. Le circuit (410, 321) d'écriture de données divise le flux reçu de données enregistrées en segments de données, dont chacun contient un nombre prédéterminé d'octets de données. Un premier code d'erreur de groupe de balayage est généré en fonction de chaque segment de données alors qu'un second code d'erreur de groupe de balayage est généré sur plusieurs segments de données. Un code de correction d'erreurs (ECC-3) de troisième niveau est également utilisé pour protéger un groupe de balayage complet (700) plutôt que de protéger des données en fonction de chaque octet. Le générateur (805) de code de correction

d'erreur de troisieme niveau produit un code d'erreur sur un nombre predetermine de groupes de balayage (700) inscrits en sequence afin de permettre a l'organe de commande (350) de reconstruire un groupe de balayage entier (700) si l'integrite de donnees est compromise.

Fulltext Availability:
Detailed Description

Detailed Description

... two
parallel write paths (402-* to 410-f1, The data that
is transf erred f rom buf f er 401 through head switch 4 11
is written into a field memory array 402 so that the
data can continuously be supplied to rotating write
heads 321,
outer ECC Encoder
While the data is being read in 128 byte segments
into field memory array 402, it is also applied to the
input of outer ECC encode circuit 403 to produce 8
check bytes of a Reed Solomon error correcting code...

?

File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Apr
(c)2004 Info.Sources Inc
File 2:INSPEC 1969-2004/May W1
(c) 2004 Institution of Electrical Engineers
File 6:NTIS 1964-2004/May W2
(c) 2004 NTIS, Intl Cpyrght All Rights Res
File 8:Ei Compendex(R) 1970-2004/May W1
(c) 2004 Elsevier Eng. Info. Inc.
File 34:SciSearch(R) Cited Ref Sci 1990-2004/May W2
(c) 2004 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2004/Apr
(c) 2004 ProQuest Info&Learning
File 65:Inside Conferences 1993-2004/May W2
(c) 2004 BLDSC all rts. reserv.
File 94:JICST-EPlus 1985-2004/Apr W3
(c)2004 Japan Science and Tech Corp(JST)
File 95:TEME-Technology & Management 1989-2004/Apr W4
(c) 2004 FIZ TECHNIK
File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Apr
(c) 2004 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/May 13
(c) 2004 The Gale Group
File 144:Pascal 1973-2004/May W1
(c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
(c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
(c) 2003 EBSCO Pub.
File 266:FEDRIP 2004/Mar
Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 483:Newspaper Abs Daily 1986-2004/May 10
(c) 2004 ProQuest Info&Learning
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
(c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
(c)2001 ProQuest Info&Learning

Set	Items	Description
S1	1144	JEDEC OR (JT OR JOINT) ()ELECTRONIC?? ? ()DEVICE? ? ()ENGINE- ER? ? OR JESD3 ()C OR JESD ()3
S2	92323	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPL- DS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FPGAS
S3	188282	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR- OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S4	997740	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S5	5135	S4 (1W) LOGIC (1W) DEVICE? ?
S6	6017	S4 (1W) LOGIC (1N) ARRAY? ?
S7	19566	S4 (1W) GATE? ? (1W) ARRAY? ?
S8	136	S4 () (IC OR ICS)
S9	566	S4 (1W) INTEGRATED () CIRCUIT???? ?
S10	0	S4 (1W) ELLECTRICAL?? ? (1W) ERASE???? ? (1W) LOGIC? ?
S11	46	GENERIC (1W) ARRAY? ? (1W) LOGIC? ?
S12	11749	(READONLY OR READ () ONLY) (1W) (MEMORY? OR MEMORIES OR STORAG- E?)
S13	2156949	STORAGE? OR STORE? ? OR STORING OR MEMORY? OR MEMORIES OR - PRESTOR??? ?
S14	73414	S13 (3N) (FIELD? ? OR SPACE? ? OR AREA? ? OR REGION? ? OR SE-

CTOR? ? OR ZONE? ? OR SECTION? ? OR PART OR PARTS OR PORTION?
?)

S15 144126 S13(3N)DATA

S16 60996 S13(3N)(PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PRO-
PERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATT-
RIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR -
FEATURES)

S17 0 S4(1W)ELECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?

S18 16249 BINARY(1W)TREE? ? OR HUFFMAN

S19 15626431 PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PROPERTY? OR
PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATTRIBUTES OR
BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR FEATURES

S20 199082 S19(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACK-
ED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDU-
C? OR REDN? ? OR DIMINISH?)

S21 183048 S19(3N)(REDUC??? ? OR REDUCTION? OR DECREAS? OR DECREMENT?
OR ENCOD??? ? OR CODIFY? OR CODIFIE? OR CODIFIC? OR INCOD??? -
?)

S22 1719777 NONCONFORM? OR INCOMPAT? OR INOPERA? OR UNUSUAL OR DYSFUNC-
T? OR INCOMPLETE? OR DEVIA? OR IRREGULAR? OR EXCEPTION? ? OR -
DISTORT?

S23 2221171 DISFUNCT? OR UNCONFORM? OR UNCOMPAT? OR UNCOMPLET? OR DISC-
REPAN? OR DEGRAD? OR DISPARAT? OR BUG? ? OR ERROR? ? OR CORRU-
PT? OR INVALID?

S24 8821503 MISTAK? OR FAIL???? ? OR PROBLEM? ? OR FAULT? OR DEFECT? OR
DEFICIEN? OR ABNORMA? OR DAMAG? OR FLAW? OR IMPAIR?

S25 325081 ABERRA? OR MALFUNCTI? OR IMPERFECT?

S26 50542 DEBUG? OR DE()BUG???? ? OR ECC OR ECCS OR EDAC OR EDACS

S27 54 S4(1W)ELECTRICAL?? ?(1W)ERAS?(1W)LOGIC? ?

S28 495700 S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH-
EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PRO-
BING? OR SEARCH? OR SURVEY?)

S29 731300 S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? -
OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR
LOCAT? OR REVIEW?)

S30 452967 S22:S25(3N)(DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENT-
IFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECO-
GNIS? OR RECOGNIZ? OR RECOGNIT?)

S31 560349 S22:S25(3N)(INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR
SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT???
? OR FILTER??? ?)

S32 170520 DATA(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PAC-
KED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR RED-
UC? OR REDN? ? OR DIMINISH?)

S33 18470 DATA(3N)(DECREAS? OR DECREMENT? OR ENCOD???? ? OR CODIFY? -
OR CODIFIE? OR CODIFIC? OR INCOD??? ?)

S34 137 (S2:S3 OR S5:S12 OR S27) AND S1

S35 9694 (S2:S3 OR S5:S12 OR S27) AND S14:S16

S36 569 S35 AND (S18 OR S20:S21 OR S32:S33)

S37 26 S36 AND S28:S31

S38 4 S36 AND S26

S39 0 S36 AND S1

S40 8 S35 AND S1

S41 37 S37:S40

S42 5 S41/2002:2004

S43 29 S41 NOT S40

S44 27 RD (unique items)

44/9/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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6853671 INSPEC Abstract Number: C2001-04-5220-006

Title: A reliable LZ data compressor on reconfigurable coprocessors

Author(s): Huang, W.-J.; Saxena, N.; McCluskey, E.J.

Author Affiliation: Center for Reliable Comput., Stanford Univ., CA, USA

Conference Title: Proceedings 2000 IEEE Symposium on Field-Programmable Custom Computing Machines (Cat. No.PR00871) p.249-58

Editor(s): Hutchings, B.L.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 2000 **Country of Publication:** USA x+348 pp.

ISBN: 0 7695 0871 5 **Material Identity Number:** XX-2001-00189

U.S. Copyright Clearance Center Code: 0 7695 0871 5/2000/\$10.00

Conference Title: Proceedings 2000 IEEE Symposium on Field-Programmable Custom Computing Machines

Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Archit

Conference Date: 17-19 April 2000 **Conference Location:** Napa Valley, CA, USA

Language: English **Document Type:** Conference Paper (PA)

Treatment: Practical (P)

Abstract: Data compression techniques based on the Lempel-Ziv (LZ) algorithm are widely used in a variety of applications, especially in communications and data storage. However, since the LZ algorithm involves a considerable amount of parallel comparisons, it may be difficult to achieve a very high throughput using software approaches on general-purpose processors. In addition, error propagation due to single-bit transient errors during LZ compression causes a data integrity problem. We present an implementation of LZ data compression on reconfigurable hardware with concurrent error detection for high performance and reliability. Our approach achieves 100 Mbps throughput using four Xilinx 4036XLA FPGA chips. We also present an inverse comparison technique for LZ compression to guarantee data integrity with less area overhead than traditional systems based on duplication. The resulting execution time overhead and compression ratio degradation due to concurrent error detection is also minimized. (20 Refs)

Subfile: C

Descriptors: coprocessors; data compression; data integrity; error detection; field programmable gate arrays; reconfigurable architectures

Identifiers: LZ data compressor; reconfigurable coprocessors; data compression techniques; Lempel-Ziv algorithm; throughput; general-purpose processors; error propagation; single-bit transient errors; data integrity; error detection; high performance; Xilinx FPGA chips; execution time overhead; compression ratio degradation; reliability; 100 Mbit/s

Class Codes: C5220 (Computer architecture); C5130 (Microprocessor chips); C1260 (Information theory); C6130 (Data handling techniques); C5120 (Logic and switching circuits)

Numerical Indexing: bit rate 1.0E+08 bit/s

Copyright 2001, IEE

44/9/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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03494899 INSPEC Abstract Number: B89067767, C89066970

Title: Built-in test of CMOS state machines with realistic faults: a system perspective

Author(s): Katoozi, M.; Soma, M.

Author Affiliation: Seattle Silicon Corp., Bellevue, WA, USA

Conference Title: Proceedings of the IEEE 1989 Custom Integrated Circuits

Conference (Cat. No.89CH2671-6) p.22.5/1-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 790 pp.
U.S. Copyright Clearance Center Code: CH2671-6/89/0000-0139\$01.00
Conference Sponsor: IEEE
Conference Date: 15-18 May 1989 Conference Location: San Diego, CA,
USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: A built-in test system that is capable of parallel testing all combinational and sequential arrays on a CMOS chip is presented. The system is based on a recently introduced tristate multiplexing design for programmable and register logic arrays and requires minimal on-chip test storage and silicon area overhead. The test procedure is tailored to the detection of real mask defects in the layout of the array. The system also uses simple and economical data compaction circuit that provides a good fault coverage while not precluding the use of more sophisticated data compactors. (24 Refs)

Subfile: B C

Descriptors: CMOS integrated circuits; combinatorial circuits; logic arrays; logic testing; sequential circuits

Identifiers: programmable logic arrays ; PLA ; logic testing; real mask defects detection ; combinational arrays; CMOS state machines; built-in test system; parallel testing; sequential arrays; CMOS chip; tristate multiplexing design; register logic arrays; on-chip test storage; test procedure; layout; data compaction circuit

Class Codes: B1265B (Logic circuits); B2570D (CMOS integrated circuits); C5210 (Logic design methods)

44/9/7 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

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02844497 INSPEC Abstract Number: C87022597

Title: Data structure of the compact disk- read - only memory system

Author(s): Sako, Y.; Suzuki, T.

Author Affiliation: Inf. Syst. Res. Center, Sony Corp., Tokyo, Japan

Journal: Applied Optics vol.25, no.22 p.3996-4000

Publication Date: 15 Nov. 1986 Country of Publication: USA

CODEN: APOPAI ISSN: 0003-6935

U.S. Copyright Clearance Center Code: 0003-6935/86/223996-05\$02.00/0

Language: English Document Type: Journal Paper (JP)

Treatment: New Developments (N); Practical (P)

Abstract: The compact disk- read - only memory (CD- ROM) system, based on the digital audio compact disk system, is designed as a data storage system for computers by Sony and Philips. This paper outlines the CD- ROM system and describes the data structure (user data, 2K bytes), especially a new error correction system. The performance of this new correction system is good enough to store digital data in the CD- ROM . Two hundred disks in actual use were checked and no uncorrectable error data were found. In addition, this paper summarizes production of CD- ROM disks. (2 Refs)

Subfile: C

Descriptors: CD- ROMs ; video and audio discs

Identifiers: computer data storage system; optical stripe; compact disk- read - only memory system; digital audio compact disk system; Sony ; Philips; CD- ROM system; data structure; error correction system; digital data; production; 2 kbytes

Class Codes: C5320K (Optical storage)
Numerical Indexing: memory size 2.0E+03 Byte

44/9/10 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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06445438 E.I. No: EIP03297543912

Title: **A fault tolerant hardware based file system manager for solid state mass memory**

Author: Cardarilli, G.C.; Ottavi, M.; Pontarelli, S.; Re, M.; Salsano, A.
Corporate Source: Department of Electronic Engineering University of Rome Tor Vergata, 00133-Rome, Italy

Conference Title: Proceedings of the 2003 IEEE International Symposium on Circuits and Systems

Conference Location: Bangkok, Thailand Conference Date: 20030525-20030528

Sponsor: IEEE Circuits and Systems Society; Mahanakorn University of Technology

E.I. Conference No.: 61139

Source: Proceedings - IEEE International Symposium on Circuits and Systems v 5 2003. p V649-V652 (IEEE cat n 03CH37430)

Publication Year: 2003

CODEN: PICSDI ISSN: 0271-4310

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0307W3

Abstract: In this paper the hardware implementation of a file system manager for a fault tolerant Solid State Mass Memory (SSMM) is presented. A hardware implementation of the file system manager implies the following advantages: ad hoc fault tolerant design and graceful degradation capability. The former means developing special fault tolerant hardware for each file system basic function (read, write and delete). For each function different fault tolerant techniques have been applied by considering the impact of different faults on the architecture reliability. Also the area overhead introduced by the chosen fault tolerant technique has been evaluated. Graceful degradation is obtained in terms of data connection reconfiguration and reduced functionality set. We exploited the modularity of the design to implement a distributed file system by means of local handlers on each memory module connected to a dynamic routing module. The file system manager has been used in a SSMM oriented to satellite applications. An FPGA implementation for the complete SSMM has been obtained in order to evaluate the performances and reliability of the SSMM architecture and in particular of the file system manager. 14 Refs.

Descriptors: Data storage equipment; Fault tolerant computer systems; Parallel processing systems; Error correction; Computer architecture; Data transfer; Data acquisition; Data handling; Space applications; Interfaces (computer); Data flow analysis

Identifiers: Solid state mass memory (SSMM)

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 723.2 (Data Processing); 722.2 (Computer Peripheral Equipment); 723.1 (Computer Programming)
722 (Computer Hardware); 721 (Computer Circuits & Logic Elements); 723 (Computer Software, Data Handling & Applications); 656 (Space Flight)
72 (COMPUTERS & DATA PROCESSING); 65 (AEROSPACE ENGINEERING)

44/9/11 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04567102 E.I. No: EIP96123431103

Title: Error characteristics of read - only - memory versus write-once-read-many compact discs: CD- ROM versus CD-WORM

Author: Tehranchi, Babak; Howe, Dennis G.

Corporate Source: Univ of Arizona, Tucson, AZ, USA

Source: Applied Optics v 35 n 29 Oct 10 1996. p 5831-5838

Publication Year: 1996

CODEN: APOPAI ISSN: 0003-6935

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9701W4

Abstract: Some of the parameters that are used to assess the reliability of data recovered from CD's are described. A brief description of the error-measurement procedure is provided, and the burst- and gap-length distributions that were obtained from the examination of eight CD-WORM's and eight CD- ROM 's are presented. These results correspond to a byte-by-byte examination of the serial stream of data that is recorded contiguously on a disc track. A report of an alternative representation for the gap-length probabilities is provided. The measured error statistics for hard and soft errors are then presented, and their significance is discussed. Finally, a quantitative means for determining the confidence limits in the estimation of the measured error-probability values is provided. The error-measurement results presented in this paper can ultimately be used to determine the reliability of the data delivered to users of the various types of CD. 11 Refs.

Descriptors: Optical data storage ; Compact disks; Error detection ; Probability; Error correction; Codes (symbols); Error analysis ; Integral equations

Identifiers: Write once read many compact discs; Error bursts; Error measurement; Confidence limits; Cross interleaved Reed-Solomon code; Good data gaps

Classification Codes:

752.3.1 (Sound Reproduction Equipment)

722.1 (Data Storage, Equipment & Techniques); 752.3 (Sound Reproduction); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 922.1 (Probability Theory); 723.2 (Data Processing); 921.2 (Calculus)

722 (Computer Hardware); 752 (Sound Equipment & Systems); 721 (Computer Circuits & Logic Elements); 922 (Statistical Methods); 723 (Computer Software); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 75 (ACOUSTICAL TECHNOLOGY); 92 (ENGINEERING MATHEMATICS)

44/9/12 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04375249 E.I. No: EIP96023035859

Title: Is there a CD-R media problem?

Author: Cochrane, Katherine

Corporate Source: CD-Info Co, Inc, Huntsville, AL, USA

Source: CD-ROM Professional v 9 n 2 Feb 1996. 9pp

Publication Year: 1996

CODEN: CRPFEX ISSN: 1049-0833

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 9605W5

Abstract: There is currently a free-floating anxiety in industry and business circles about whether the CD-Recordable discs is being used are any good. Several criteria go into evaluating disc usefulness: readability, compatibility with recorders and players, and expected lifespan. Results amassed in a series of tests performed by One-Off CD Shops International between early 1993 and mid-1995 on a variety of disc brands and types shed light on the topic, even though the tests were done only to evaluate readability of recorded discs, and not media longevity or suitability of specific brands or types for use on every system. However, the methodological rigor the narrow focus afforded yielded considerable data that bodes well for the effectiveness of current disc-evaluating mechanisms. Not every question has been answered by any means, but one finding is clear: worry about the quality of CD-R media seems largely unfounded.

Descriptors: CD- ROM ; Computer testing; Compact disks; Data recording; Digital storage ; Standards; Digital to analog conversion; Error detection ; Error correction; Performance

Identifiers: CD-recordable discs; Readability testing; Replicated discs; CD-digital audio; Troubleshooting; Digital errors; Analog errors; Physical errors; Logical errors; Error rates

Classification Codes:

752.3.1 (Sound Reproduction Equipment)

722.1 (Data Storage, Equipment & Techniques); 752.3 (Sound Reproduction); 723.2 (Data Processing); 722.4 (Digital Computers & Systems)

722 (Computer Hardware); 752 (Sound Equipment & Systems); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING); 75 (ACOUSTICAL TECHNOLOGY)
? t44/9/16-17,19-20,23

44/9/16 (Item 8 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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01338158 E.I. Monthly No: EI8303017191 E.I. Yearly No: EI83023041
Title: ROM EMULATOR FOR THE CONNECTION OF THE PROM PROGRAMMER UPP103.
Author: Storandt, Steffen
Corporate Source: Siemens, Munich, Ger
Source: Siemens Components v 17 n 5 Oct 1982 p 154-155
Publication Year: 1982
CODEN: SICOD5
Language: ENGLISH
Journal Announcement: 8303

Abstract: Programs and constants for Random Access Memories (ROMs) usually are developed by means of a microcomputer development system, for instance the Siemens microcomputer development systems SME. The user hardware is connected with the emulation and test adapter (ETA). The programs and the constants are stored in the development system. The program steps can be monitored on the CRT, failure recognized and eliminated. The elaboration of a program or of constants using an ETA may be limited or not possible. A low-cost and time saving auxiliary equipment for SME is presented that features reduced programming time, erasing time savings for the erasable programmable ROM (EPROM), no replugging of the EPROM from programming equipment to hardware, and no wear due to frequent erasing and programming actions.

Descriptors: DATA STORAGE , DIGITAL--*Random Access; COMPUTER PROGRAMMING--Monitoring; COMPUTERS, MICROPROCESSOR--Applications
Identifiers: PROGRAMMABLE ROM (PROM); EMULATION AND TEST ADAPTER

(DTA)

Classification Codes:

722 (Computer Hardware); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING)

44/9/17 (Item 9 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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01194934 E.I. Monthly No: EI8209076896 E.I. Yearly No: EI82025918

Title: SMART CONTROLLER MEETS DISK-MEMORY CHALLENGE.

Author: Chu, Paul; Kitson, Brad; Tabler, Otis

Corporate Source: Adv Micro Devices Inc, Sunnyvale, Calif, USA

Source: Electronic Design v 30 n 13 Jun 24 1982 p 133-138, 140, 142

Publication Year: 1982

CODEN: ELODAW ISSN: 0013-4872

Language: ENGLISH

Journal Announcement: 8209

Abstract: A smart controller can conserve disk storage space through its data compression function and increase access speed through request queueing. Both functions, as well as read and write routines, are microcoded into the controller's logic and stored in registered PROM. An intelligent controller can detect and correct burst errors - impractical tasks at best for the host computer - ensuring that data are transferred accurately and reliably. High-speed data transfer, supporting firmware, and extensive error detection and correction capabilities characterize a VLSI disk controller which is described. The latter was designed to keep pace with read/write circuits and head technologies.

Descriptors: DATA STORAGE, MAGNETIC--*Disk; INTEGRATED CIRCUITS--Very Large Scale Integration

Classification Codes:

721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 713 (Electronic Circuits); 714 (Electronic Components)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

44/9/19 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

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1083855 ORDER NO: AAD90-00260

BUILT-IN TEST OF CMOS STRUCTURED LOGIC WITH REALISTIC FAULT MODELS

Author: KATOOZI, MEHDI

Degree: PH.D.

Year: 1989

Corporate Source/Institution: UNIVERSITY OF WASHINGTON (0250)

CHAIRPERSON: MANI SOMA

Source: VOLUME 50/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 3624. 115 PAGES

Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL

Descriptor Codes: 0544

Built-in test has surfaced as a solution to the costly test generation and data storage problems. Structured designs such as programmable and storage logic arrays (PLA and SLA) are also desirable alternatives to random logic implementations of integrated circuits due to their ease of synthesis. Structured design for built-in testability is the main objective of this dissertation.

Yield analysis studies indicate that testing arrays for classical

faults does not provide sufficient coverage of real physical defects. Another shortcoming of the existing test techniques is their loss of practicality for large arrays due to a large hardware overhead. Testing SLAs is further complicated by their feedback. Functional test is time consuming and requires the transformation of the state machine to a testable one with a different state table. Functional test of the transformed machine does not always assure the correct functionality of the original one. Furthermore, faults that give rise to extraneous transitions are not detected because functional test only checks the transitions in the original design.

This thesis presents a new design for structural testing of CMOS arrays. Tri-state capability is used to allow testing of the SLA with exactly the same overhead as the PLA regardless of feedback. The overhead is lower than the existing techniques and decreases with increased array size, making the technique practical for large arrays. Real faults resulting from mask **defects** are **analyzed** for their electrical effect on the circuit. Special features are incorporated into the layout to eliminate or provide tolerance to undetectable **faults**. Requirements for **detecting** the remaining **faults** are derived and met by adding appropriate product lines. **Deficiencies** in functional **test** of storage elements are identified and eliminated by layout practices that reduce the probability of undetectable **faults**.

A built-in **test** technique is proposed that accommodates the parallel testing of arrays. This scheme requires minimal on-chip test **storage**, and a simple **data compaction** circuit. The testable array is implemented in double metal, CMOS technology. Simulation indicates no performance penalty associated with the test circuitry which stems from the fact that no extra gate delays are introduced in the input signal path.

44/9/20 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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04324443 JICST ACCESSION NUMBER: 99A0909894 FILE SEGMENT: JICST-E

Testing the SRAM-based FPGAs .

DOUMAR A (1); ITO H (1)

(1) Chiba Univ., Jpn

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report
(Institute of Electronics, Information and Communication Engineers),
1999, VOL.99,NO.250(FTS99 31-39), PAGE.43-50, FIG.7, TBL.6, REF.13

JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.08

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: This paper presents a new design for testing SRAM-based field **programmable gate arrays (FPGAs)**. The new proposed method is able to test both the configurable logic blocks(CLBs) and the interconnection networks for a wide fault model including stuck at fault, bridging fault and open fault. The proposed design is consisting on a slightly modifying the original SRAM part in **FPGA** so that it will allow the configuration data to be looped on-chip and then the test becomes easier. This method requires a very short test time comparing to the previous works. More over the off-chip memory used in the **storage** of the configurations **data** is considerably **reduced** . The application of this method on XC4000 family and ORCA shows that (relatively to that required by the previous works) the test time can be reduced by 87.2% and the required off-chip memory can be reduced by

88.6%. (author abst.)
DESCRIPTORS: **FPGA** ; SRAM; circuit test; testability; **fault detection** ;
fault diagnosis ; failure mode(reliability
BROADER DESCRIPTORS: ASIC; integrated circuit; micro circuit; RAM;
memory(computer); equipment; static memory; test; possibility; system
characteristic; characteristic; detection; diagnosis
CLASSIFICATION CODE(S): NC03040G

44/9/23 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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10337784 PASCAL No.: 92-0541244
Efficient computation of the squaring operation in modular rings
RAO P B; SKAVANTZOS A
Louisiana state univ., dep. electrical computer eng., Baton Rouge LA
70803, USA
Journal: Electronics letters, 1992, 28 (17) 1628-1630
ISSN: 0013-5194 CODEN: ELLEAK Availability: INIST-12270;
354000020452930400
No. of Refs.: 7 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: United Kingdom
Language: English
Modular arithmetic is used extensively in signal processing and in **error detecting** and correcting codes. In these applications many modulo operations are obtained using table lookup techniques. In the Letter, new and simple memory compression techniques are presented that result in significant **ROM** bit savings, to compute the squaring operation modulo m
English Descriptors: Signal processing; **Error** correcting code; **Error detecting** code; **Read only memory** (ROM); **Data reduction** ;
Arithmetics; Digital signal; **Data compression**
French Descriptors: Traitement signal; Code correcteur erreur; Code detecteur erreur; Memoire morte; Reduction donnee; Arithmetique; Signal numerique; Compression donnee

Classification Codes: 001D03F06B

File 9:Business & Industry(R) Jul/1994-2004/May 12
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File 16:Gale Group PROMT(R) 1990-2004/May 13
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File 47:Gale Group Magazine DB(TM) 1959-2004/May 13
(c) 2004 The Gale group
File 148:Gale Group Trade & Industry DB 1976-2004/May 13
(c)2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/May 13
(c) 2004 The Gale Group
File 570:Gale Group MARS(R) 1984-2004/May 13
(c) 2004 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2004/May 12
(c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/May 13
(c) 2004 The Gale Group
File 649:Gale Group Newswire ASAP(TM) 2004/May 12
(c) 2004 The Gale Group

Set	Items	Description
S1	7319	JEDEC OR (JT OR JOINT) ()ELECTRONIC?? ? ()DEVICE? ? ()ENGINE- ER? ? OR JESD3 ()C OR JESD ()3
S2	137569	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPL- DS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FGAS
S3	608138	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR- OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S4	1273243	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S5	16705	S4 (1W) LOGIC (1W) DEVICE? ?
S6	4559	S4 (1W) LOGIC (1N) ARRAY? ?
S7	12736	S4 (1W) GATE? ? (1W) ARRAY? ?
S8	720	S4 () (IC OR ICS)
S9	798	S4 (1W) INTEGRATED () CIRCUIT???? ?
S10	0	S4 (1W) ELLECTRICAL?? ? (1W) ERASE???? ? (1W) LOGIC? ?
S11	243	GENERIC (1W) ARRAY? ? (1W) LOGIC? ?
S12	17152	(READONLY OR READ () ONLY) (1W) (MEMORY? OR MEMORIES OR STORAG- E?)
S13	5133532	STORAGE? OR STORE? ? OR STORING OR MEMORY? OR MEMORIES OR - PRESTOR??? ?
S14	374487	S13 (3N) (FIELD? ? OR SPACE? ? OR AREA? ? OR REGION? ? OR SE- CTOR? ? OR ZONE? ? OR SECTION? ? OR PART OR PARTS OR PORTION? ?)
S15	330630	S13 (3N) DATA
S16	158531	S13 (3N) (PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PRO- PERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATT- RIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR - FEATURES)
S17	2	S4 (1W) ELECTRICAL?? ? (1W) ERASE???? ? (1W) LOGIC? ?
S18	9524	BINARY (1W) TREE? ? OR HUFFMAN
S19	10461252	PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PROPERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATTRIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR FEATURES
S20	159020	S19 (3N) (COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACK- ED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDU- C? OR REDN? ? OR DIMINISH?)
S21	116156	S19 (3N) (REDUC??? ? OR REDUCTION? OR DECREAS? OR DECREMENT? OR ENCOD??? ? OR CODIFY? OR CODIFIE? OR CODIFIC? OR INCOD??? - ?)

S22 1228929 NONCONFORM? OR INCOMPAT? OR INOPERA? OR UNUSUAL OR DYSFUNC-
T? OR INCOMPLETE? OR DEVIA? OR IRREGULAR? OR EXCEPTION? ? OR -
DISTORT?

S23 1137076 DISFUNCT? OR UNCONFORM? OR UNCOMPAT? OR UNCOMPLET? OR DISC-
REPAN? OR DEGRAD? OR DISPARAT? OR BUG? ? OR ERROR? ? OR CORRUP-
T? OR INVALID?

S24 6149992 MISTAK? OR FAIL???? ? OR PROBLEM? ? OR FAULT? OR DEFECT? OR
DEFICIEN? OR ABNORMA? OR DAMAG? OR FLAW? OR IMPAIR?

S25 96832 ABERRA? OR MALFUNCTI? OR IMPERFECT?

S26 120242 DEBUG? OR DE()BUG???? ? OR ECC OR ECCS OR EDAC OR EDACS

S27 151 S4(1W)ELECTRICAL?? ?(1W)ERAS?(1W)LOGIC? ?

S28 293156 S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH-
EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PRO-
BING? OR SEARCH? OR SURVEY?)

S29 204644 S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? -
OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR
LOCAT? OR REVIEW?)

S30 259187 S22:S25(3N)(DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENT-
IFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECO-
GNIS? OR RECOGNIZ? OR RECOGNIT?)

S31 275514 S22:S25(3N)(INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR
SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT???
? OR FILTER??? ?)

S32 126401 DATA(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PAC-
KED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR RED-
UC? OR REDN? ? OR DIMINISH?)

S33 16851 DATA(3N)(DECREAS? OR DECREMENT? OR ENCOD???? ? OR CODIFY? -
OR CODIFIE? OR CODIFIC? OR INCOD??? ?)

S34 769 (S2:S3 OR S5:S12 OR S27)(S)S1

S35 20538 (S2:S3 OR S5:S12 OR S27)(S)S14:S16

S36 638 S35(S)(S18 OR S20:S21 OR S32:S33)

S37 15 S36(S)S28:S31

S38 7 S36(S)S26

S39 1 S36(S)S1

S40 19 S37:S39

S41 0 S40/2002:2004

S42 13 RD S40 (unique items)

42/3,K/6 (Item 6 from file: 16)

DIALOG(R)File 16:Gale Group PROMT(R)

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01139248 Supplier Number: 41290225

ALTERA AND ATMEL EPLD SUPPORT ADDED TO TANGO-PLD

News Release, p1

April 23, 1990

Language: English Record Type: Abstract

Document Type: Magazine/Journal; Trade

ABSTRACT:

ACCEL Technologies has just released Version 1.11 of their Tango- PLD software for **programmable logic device** design. This newest version adds support for four Altera **EPLD** devices: the EP310, 320, 600 and 900 plus a device model for the 40-pin, UV-erasable Atmel V2500. This release also **features reduced memory** requirements, which permit large, complex designs without requiring expanded memory. TangoPLD now supports 109 **PAL** , **GAL** and **PEEL** devices and provides the capability of designing the industry's most popular **programmable logic devices** . Tango- **PLD** is a design compiler, logic mirvmizer and simulator combined into one easy-to-use program. It offers innovative features, speed and

simplicity. Some of Tango- PLD0 's features include: separation of the logic design phase from the device selection phase, so that the designer can refine and test a logic design prior to deciding which PLD to use; multiple device simulation, allowing a complex design consisting of several interconnected PLDs to be tested with a single set of test vectors; test vector coverage analysis; the...

...blocks and groups (indexed variables) for concise design descriptions and test vector generation; industry-standard JEDEC files for component programming; unique cross reference and source listing files for source-level debugging ; and faster simulation and logic minimization than other popular PLD programs, which speeds up the overall design process.

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File 696:DIALOG Telecom. Newsletters 1995-2004/May 12
(c) 2004 The Dialog Corp.
File 15:ABI/Inform(R) 1971-2004/May 13
(c) 2004 ProQuest Info&Learning
File 98:General Sci Abs/Full-Text 1984-2004/May
(c) 2004 The HW Wilson Co.
File 484:Periodical Abs Plustext 1986-2004/May W2
(c) 2004 ProQuest
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/May 13
(c) 2004 PR Newswire Association Inc
File 635:Business Dateline(R) 1985-2004/May 13
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File 610:Business Wire 1999-2004/May 13
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File 369:New Scientist 1994-2004/May W1
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File 370:Science 1996-1999/Jul W3
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(c) 2004 McGraw-Hill Co. Inc
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File 647:CMP Computer Fulltext 1988-2004/May W1
(c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/May W1
(c) 2004 IDG Communications

Set	Items	Description
S1	2976	JEDEC OR (JT OR JOINT)()ELECTRONIC?? ?()DEVICE? ? ()ENGINE-ER? ? OR JESD3()C OR JESD()3
S2	173824	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPLDS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FPGAS
S3	363982	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR-OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S4	784518	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S5	7568	S4(1W)LOGIC(1W)DEVICE? ?
S6	556	S4(1W)LOGIC(1N)ARRAY? ?
S7	5904	S4(1W)GATE? ?(1W)ARRAY? ?
S8	363	S4() (IC OR ICS)
S9	473	S4(1W)INTEGRATED()CIRCUIT???? ?
S10	0	S4(1W)ELLECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S11	156	GENERIC(1W)ARRAY? ?(1W)LOGIC? ?
S12	5599	(READONLY OR READ()ONLY) (1W) (MEMORY? OR MEMORIES OR STORAG-E?)
S13	3657602	STORAGE? OR STORE? ? OR STORING OR MEMORY? OR MEMORIES OR - PRESTOR??? ?
S14	232848	S13(3N) (FIELD? ? OR SPACE? ? OR AREA? ? OR REGION? ? OR SE-CTOR? ? OR ZONE? ? OR SECTION? ? OR PART OR PARTS OR PORTION? ?)
S15	173023	S13(3N)DATA
S16	82206	S13(3N) (PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PRO-PERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATT-RIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR -

FEATURES)

S17 1 S4(1W)ELECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?

S18 8195 BINARY(1W)TREE? ? OR HUFFMAN

S19 9475671 PARAMETER? OR PARAMETRE? OR VALUE OR VALUES OR PROPERTY? OR PROPERTIES OR CHARACTERISTIC? ? OR ATTRIBUTE OR ATTRIBUTES OR BOUND? ? OR CRITERIA? OR CRITERION? OR FEATURE OR FEATURES

S20 115319 S19(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACK-ED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDUC? OR REDN? ? OR DIMINISH?)

S21 102311 S19(3N)(REDUC??? ? OR REDUCTION? OR DECREAS? OR DECREMENT? OR ENCOD??? ? OR CODIFY? OR CODIFIE? OR CODIFIC? OR INCOD??? - ?)

S22 1515521 NONCONFORM? OR INCOMPAT? OR INOPERA? OR UNUSUAL OR DYSFUNCTION? OR INCOMPLETE? OR DEVIA? OR IRREGULAR? OR EXCEPTION? ? OR - DISTORT?

S23 1496150 DISFUNCT? OR UNCONFORM? OR UNCOMPAT? OR UNCOMPLET? OR DISCREPAN? OR DEGRAD? OR DISPARAT? OR BUG? ? OR ERROR? ? OR CORRUPT? OR INVALID?

S24 9053722 MISTAK? OR FAIL???? ? OR PROBLEM? ? OR FAULT? OR DEFECT? OR DEFICIEN? OR ABNORMA? OR DAMAG? OR FLAW? OR IMPAIR?

S25 120812 ABERRA? OR MALFUNCTI? OR IMPERFECT?

S26 54303 DEBUG? OR DE()BUG???? ? OR ECC OR ECCS OR EDAC OR EDACS

S27 113 S4(1W)ELECTRICAL?? ?(1W)ERAS?(1W)LOGIC? ?

S28 277866 S22:S25(3N)(DETECT? OR DET? ? OR DETERMIN? OR CHECK? OR CH-EQU? OR DX OR TRACE? ? OR TRACING OR SEEK? OR PROBE? ? OR PROBING? OR SEARCH? OR SURVEY?)

S29 231537 S22:S25(3N)(DISCRIMINAT? OR ANALYS? OR ANALYT? OR ANALYZ? - OR ASSESS? OR SELFDIAGNOS? OR SELFTEST? OR BIST OR EXAMIN? OR LOCAT? OR REVIEW?)

S30 269666 S22:S25(3N)(DIAGNOS? OR IDENTIFY? OR IDENTIFIE? ? OR IDENTIFIC? OR SCREEN? OR APPRAIS? OR EVALUAT? OR SENS??? ? OR RECOGNIS? OR RECOGNIZ? OR RECOGNIT?)

S31 236769 S22:S25(3N)(INSPECT? OR MONITOR? OR TRACK? OR TEST??? ? OR SCAN OR SCANS OR SCANNED OR SCANN??? ? OR FILTR? OR DETECT??? ? OR FILTER??? ?)

S32 64456 DATA(3N)(COMPRESS???? ? OR COMPACT???? ? OR PACK? ? OR PACKED OR PACKING OR MINIMIZ? OR MINIMIS? OR CONDENS??? ? OR REDUC? OR REDN? ? OR DIMINISH?)

S33 9487 DATA(3N)(DECREAS? OR DECREMENT? OR ENCOD???? ? OR CODIFY? - OR CODIFIE? OR CODIFIC? OR INCOD??? ?)

S34 247 (S2:S3 OR S5:S12 OR S27)(S)S1

S35 7488 (S2:S3 OR S5:S12 OR S27)(S)S14:S16

S36 218 S35(S)(S18 OR S20:S21 OR S32:S33)

S37 5 S36(S)S28:S31

S38 0 S36(S)S1

S39 2 S36(S)S26

S40 6 S37:S39

S41 5 RD (unique items)

41/3,K/3 (Item 1 from file: 20)
 DIALOG(R)File 20:Dialog Global Reporter
 (c) 2004 The Dialog Corp. All rts. reserv.

23392952 (USE FORMAT 7 OR 9 FOR FULLTEXT)
SystemBIST IP enables system-wide Embedded Test and Programmable Logic Configuration
 BUSINESS WIRE
 June 17, 2002
 JOURNAL CODE: WBWE LANGUAGE: English RECORD TYPE: FULLTEXT
 WORD COUNT: 890

... FLASH for test and configuration memory --Small FLASH memory requirements due to test and configuration **data** re-use and **compression**
--Reduced PCB parts cost and area for programming **FPGAs** . --Verification and fast downloads of configuration and test files using Eclipse(TM) tool
--Support for...

... intellitech.com for more information. About Intellitech: Intellitech is the technology leader in scan-based **debug** and test solutions for SoC (System-on-a-Chip), ICs, PCBs and Systems. Intellitech's TEST-IP(TM) family provides patent pending infrastructure IP that enables embedded test, **debug** and configuration of ICs, PCBs and Systems. Intellitech's proprietary solutions enable customers to build...

... Diagnostic and Test tools to provide a powerful combination of hardware and software tools for **debug** analysis and test validation, prior to embedding into the customer's product. Intellitech is focused...

... the company has been successful in introducing new solutions based on IEEE 1149.1 configuration, **debug** and test technology. Intellitech's customer base ranges from companies providing the latest networking products...

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File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200429
(c) 2004 Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2004/May W01
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040506,UT=20040429
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	98	AU='GREEN D'
S2	89	AU='GREEN D J'
S3	24	AU='GREEN DAVID'
S4	65	AU='GREEN DAVID J':AU='GREEN DAVID JOHN'
S5	52	AU='PAK S'
S6	1	AU='PAK S Y'
S7	12	AU='NAN F'
S8	0	S1:S4 AND S5:S7
S9	440	JEDEC OR (JT OR JOINT)()ELECTRONIC?? ?()DEVICE? ? ()ENGINE- ER? ? OR JESD3()C OR JESD()3
S10	54631	PLD OR PLDS OR FPLD OR FPLDS OR PAL OR PALS OR EPLD OR EPL- DS OR PLA OR PLAS OR PROM OR PROMS OR SPLD OR SPLDS OR CPLD - OR CPLDS OR FPGA OR FGAS
S11	304330	ROM OR ROMS OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR UVR- OM OR UVROMS OR PEEL OR PEELS OR GAL OR GALS
S12	259535	PROGRAMABLE OR PROGRAMMABLE OR PROGRAMED OR PROGRAMMED OR - PROGRAMING OR PROGRAMMING
S13	6033	S12(1W)LOGIC(1W)DEVICE? ?
S14	4845	S12(1W)LOGIC(1N)ARRAY? ?
S15	7113	S12(1W)GATE? ?(1W)ARRAY? ?
S16	219	S12() (IC OR ICS)
S17	1046	S12(1W)INTEGRATED()CIRCUIT???? ?
S18	0	S12(1W)ELLECTRICAL?? ?(1W)ERASE???? ?(1W)LOGIC? ?
S19	78	GENERIC(1W)ARRAY? ?(1W)LOGIC? ?
S20	53930	(READONLY OR READ()ONLY)(1W)(MEMORY? OR MEMORIES OR STORAG- E?)
S21	41	S12(1W)ELECTRICAL?? ?(1W)ERAS?(1W)LOGIC? ?
S22	339	S1:S7
S23	0	S22 AND S9
S24	9	S22 AND (S10:S11 OR S13:S21)

24/TI/1 (Item 1 from file: 350)
DIALOG(R)File 350:(c) 2004 Thomson Derwent. All rts. reserv.

Digital video segment identification method in entertainment system,
involves associating approximated frames of digital video record until
preset percentage of video record play back time is taken by associated
commercials

24/TI/2 (Item 2 from file: 350)
DIALOG(R)File 350:(c) 2004 Thomson Derwent. All rts. reserv.

Device specification creating method e.g. for silicon device, involves
polymorphing base class representing the rules for programmable die
according to filtered device definitions

24/TI/3 (Item 3 from file: 350)
DIALOG(R)File 350:(c) 2004 Thomson Derwent. All rts. reserv.

Prepn. of combustible gas, charcoal and tar by using waste plate as raw material.

24/TI/4 (Item 4 from file: 350)
DIALOG(R)File 350:(c) 2004 Thomson Derwent. All rts. reserv.

A-D converter scheduling system for input-data sampling - synchronises sampling with process controller using adaptive scheduling

24/TI/5 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2004 WIPO/Univentio. All rts. reserv.

DUAL STAGE INFLATOR WITH EXTENDED GAS DELIVERY FOR A VEHICULAR AIRBAG SYSTEM
CONFLEUR A DEUX ETAGES AVEC DISTRIBUTION ETENDUE DE GAZ POUR UN SYSTEME D'AIRBAG DE VEHICULE

24/TI/6 (Item 2 from file: 349)
DIALOG(R)File 349:(c) 2004 WIPO/Univentio. All rts. reserv.

DUAL FLOW INFLATOR FOR A VEHICULAR AIRBAG SYSTEM
CONFLEUR A FLUX DOUBLE POUR SYSTEME D'AIRBAGS DE VEHICULES

24/TI/7 (Item 3 from file: 349)
DIALOG(R)File 349:(c) 2004 WIPO/Univentio. All rts. reserv.

APPARATUS FOR SPECTROPHOTOMETRY AND METHOD OF OBTAINING SPECTROPHOTOMETRICAL INFORMATION
APPAREIL DE SPECTROPHOTOMETRIE ET MODE DE RECUEIL DE L'INFORMATION SPECTROPHOTOMETRIQUE

24/TI/8 (Item 4 from file: 349)
DIALOG(R)File 349:(c) 2004 WIPO/Univentio. All rts. reserv.

PRESSURE-MEDIATED BINDING OF BIOMOLECULAR COMPLEXES
ASSOCIATION PAR PRESSION DE COMPLEXES BIOMOLECULAIRES

24/TI/9 (Item 5 from file: 349)
DIALOG(R)File 349:(c) 2004 WIPO/Univentio. All rts. reserv.

REPEATER INFORMATION BASE FOR SNMP NETWORK MANAGEMENT STATISTICS ACCUMULATION
BASE D'INFORMATION DE REPETEUR POUR AIDER A L'ACCUMULATION DE STATISTIQUES ET DE DONNEES DE GESTION DE RESEAU, OBTENUES PAR UN PROTOCOLE DE GESTION DE RESEAU SIMPLE

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